User's Manual

EBC5612 Series

All-in-One Tualatin Pentium III/Celeron Single Board with LCD, LVDS, AC97 Audio, IEEE-1394, Dual 10/100Base-Tx Ethernet Interfaces, & 4COMs

3rd Ed. – 4 April 2003

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1. Collect all the information about the problem encountered. (For example, CPU type and speed, BCM products model name, hardware & BIOS revision number, other hardware and software used, etc.) Note anything abnormal and list any on-screen messages you get when the problem occurs.

2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information readily available.

3. If your product is diagnosed as defective, obtain an RMA (return material authorization) number from your dealer. This allows us to process your good return more quickly.

4. Carefully pack the defective product, a complete Repair and Replacement Order Card and a photocopy proof of purchase date (such as your sales receipt) in a shippable container. A product returned without proof of the purchase date is not eligible for warranty service.

5. Write the RMA number visibly on the outside of the package and ship it prepaid to your dealer.

Packing List

Before you begin installing your single board, please make sure that the following materials have been shipped:

- 1 EBC5612 series All-in-One Tualatin Pentium III/Celeron Computing Module
- 1 Quick Installation Guide
- 1 CD-ROM contains the followings:
  - User's Manual (this manual in PDF file)
  - Ethernet driver and utilities
  - VGA drivers and utilities
  - Audio drivers and utilities
  - Latest BIOS (as of the CD-ROM was made)

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

Document Amendment History

Revision	Date	By	Comment
1st	Aug. 2002.	Steven Yen	Initial Release
2nd	Dec. 2002.	Steven Yen	1. Correct J1 & J3 description (3.6.1) 2. Correct measurement drawing
3RD	Apr. 2003.	Philip Chang	1. Correct the Jumper & Connector layout at P.18 2. Correct the connector pitch of USB1 at P.20. 3. Correct the connector description of VR1 & VR2 at P.52. 4. Add system resource data

1. Manual Objectives

This manual describes in detail the BCM EBC5612 series Single Board.

We have tried to include as much information as possible but we have not duplicated information that is provided in the standard IBM Technical References, unless it proved to be necessary to aid in the understanding of this board.

We strongly recommend that you study this manual carefully before attempting to interface with EBC5612 series or change the standard configurations. Whilst all the necessary information is available in this manual we would recommend that unless you are confident, you contact your supplier for guidance.

Please be aware that it is possible to create configurations within the CMOS RAM that make booting impossible. If this should happen, clear the CMOS settings, (see the description of the Jumper Settings for details).

If you have any suggestions or find any errors concerning this manual and want to inform us of these, please contact our Customer Service department with the relevant details.

2. Introduction

2.1 System Overview

The EBC5612 series is a compact 5.25" CD-ROM size Single Board Computer that equips with with VIA Eden ESP6000 low-power integrated processor (EBC-5613 series only), TwisterT AGPset, LCD & LVDS Interfaces, AGP 4X 3D Graphics, NTSC/PAL TV output, AC97 Audio, Dual 10/100Base-Tx Ethernet, IEEE1394 interfaces.

The EBC5612 series is equipped with a Universal Socket 370 supports Intel FC-PGA/FC-PGA2 Pentium III / Celeron (CopperMine and Tualatin) and VIA C3 processor with FSB up to 133MHz (EBC-5612 series only), powerful in performance while low power in system consumption. Its display is bolstered up with the chipset VT8606 Integrated Savage4 AGP4X graphics, supports 36-bit flat panel and dual-channel LVDS with a frame buffer of up to 32 MB. This makes this PC engine a perfect solution for Retail / Financial Transaction Terminals, and high-end multimedia POS / KIOSK Terminals.

Furthermore, the EBC5612 series is outstanding in a 5.25" form factors designed with dual PCI-bus Realtek 8139C 10/100Base-Tx Ethernet controllers. Making it the ideal solution for popular networking devices like Gateway, Router, Thin Server, Firewall and E-Box.

In addition, the on board IEEE1394, Zoom Video port, and NTSC/PAL TV output interface make the EBC5612 series also ideal for demanding high-end Entertainment Devices that require high integration multimedia Single Board Computer.

Other impressive features include a built-in 40-pin TFT LCD interface, the AC97 Audio, a Compact Flash socket for type I/ II Compact Flash storage card, four serial ports, one parallel port, and one 168-pin DIMM socket allowing for up to 512MB of SDRAM to be installed, and a PCI slot for future expansion.

2.2 System Specifications

General Functions

- **CPU:**
  - **EBC-5612 Series:** Universal Socket 370 supports Intel FC-PGA/FC-PGA2 Pentium III / Celeron (CopperMine and Tualatin) and VIA C3 CPU with FSB up to 133MHz
- **CPU Socket:** Intel FC-370, Socket 370
- **BIOS:** Award 256KB Flash BIOS
- **Chipset:** VIA VT8606 / VT82C686B
- **I/O Chipset:** VT82C686B / Winbond W83977EF-AW
- **Memory:** Onboard one 168-pin DIMM socket supports up to 512Mbytes SDRAM
- **Enhanced IDE:** Supports two IDE devices. Supports Ultra DMA/100 mode with data transfer rate up to 100MB/sec.
- **FDD Interface:** Supports up to two floppy disk drives, 5.25" (360KB and 1.2MB) and/or 3.5" (720KB, 1.44MB, and 2.88MB)
- **Parallel Port:** One bi-directional parallel port. Supports SPP, ECP, and EPP modes
- **Serial Port:** Three RS-232 and one RS-232/422/485 serial port. Ports can be configured as COM1, COM2, COM3, COM4, or disabled individually. (16C550 equivalent)
- **IR Interface:** Supports one IrDA Tx/Rx header
- **KB/Mouse Connector:** 8-pin (4 x 2) connector supports PS/2 keyboard and mouse
- **USB Connectors:** One 5 x 2 header onboard supports dual USB ports
- **Watchdog Timer:** Can generate a system reset. Software selectable time-out interval (32 sec. ~ 254min., 1 min./step)
- **Power Management:** Supports ATX power supply. Supports PC97, LAN wake up and modem ring-in functions. I/O peripheral devices support power saving and doze/standby/suspend modes. APM 1.2 compliant

IEEE1394 Interface

- **Chipset:** VIA VT6306 PCI 1394A Integrated Host Controller
- **IEEE1394 Interface:** Integrated 400Mbit 3-port PHY supports 3 IEEE 1394A ports

Flat Panel/CRT Interface

- **Chipset:** VIA VT8606, high performance 128-bit GUI, 3D engine
- **Display Memory:** 8/ 16 /32 MB frame buffer using system memory
- **Display Type:** Simultaneously supports CRT and flat panel (TFT/DSTN) displays. 36-bit DSTN/TFT flat panel interface with 256 gray shade support
- **Interface:** 4X AGP, Accelerator Graphics Ports 1.0 compliant
- **Display Mode:**
  - LCD panel supports up to 1280 x 1024 @ 24 bpp
  - CRT displays support up to 1280 x 1024 @ 24 bpp
- **Video Capture Port:** 20-pin YUV direct video input port onboard

TV Output Interface

- **TV Encoder:** VIA VT1621/1622
- **TV Output Interface:** Supports both RCA jack and S terminal

LVDS Interface

- **Chipset:** VIA VT8606
- **Scalable Bandwidth:** Ranging from 25 ~ 112MHz (VGA ~ SXGA) 18/36-bit one/two pixel per clock

Audio Interface

- **Chipset:** VIA VT82C686B
- **AC97 Codec:** AD1881A
- **Audio Controller:** AC97 2.0 compliant interface, Multi-stream Direct Sound and Direct Sound 3D acceleration
- **Audio Interface:** Microphone in, Line in, CD audio in, Line out

Ethernet Interface

- **Chipset:** Dual Realtek 8139C or Intel 82550/82559/82559ER PCI-bus Ethernet controllers onboard
- **Ethernet Interface:** PCI 100/10 Mbps, IEEE 802.3U compatible
- **Remote Boot-ROM:** For diskless system

SSD Interface

One CF+ socket supports Type I/II Compact Flash memory devices

Expansion Interface

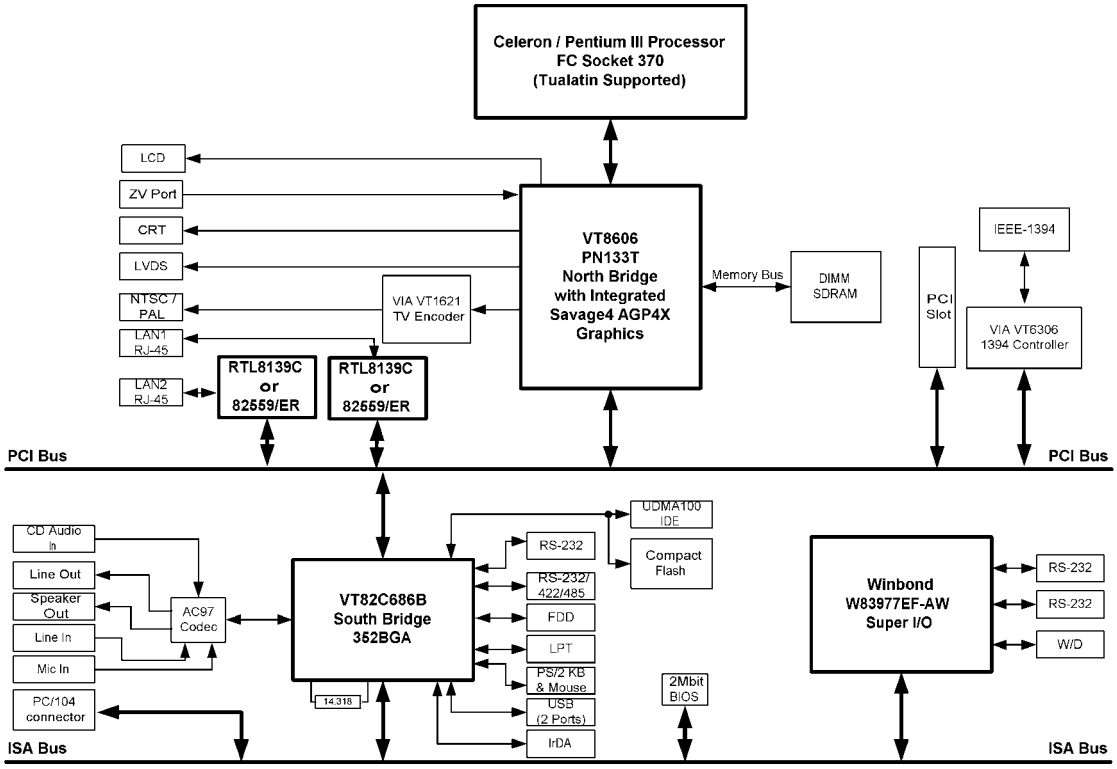
- **PC/104 Connector:** One 16-bit 104-pin connector onboard
- **PCI Slot:** One 32-bit PCI slot onboard

Mechanical and Environmental

- **Power Supply Voltage:** AT or ATX type, +5V (4.75V to 5.25V), +12V (11.4V to 12.6V)
- **Operating Temperature:** 32 to 140 °F (0 to 60 °C)
- **Board Size:** 8"(L) x 5.75"(W) (203mm x 146mm)
- **Weight:** 0.5 Kg

2.3 Architecture Overview

The following block diagram shows the architecture and main components of EBC5612.



The two key components on board are the VIA VT8606 North Bridge and VT82C686B super South Bridge. These two devices provide the ISA and PCI bus to which all the major components are attached.

The following sections provide detail information about the functions provided onboard.

2.3.1 Alternated cost effective model with VIA Eden™ Processor (EBC-5613 Series Only)

The VIA C3™ processor in Enhanced Ball Grid Array (EBGA) packaging is based upon a unique internal architecture and is manufactured using advanced 0.15μ or 0.13μ CMOS technology. The C3 architecture and process technology provide a highly compatible, high-performance, low-cost, and low-power solution for the desktop PC, notebook, and Internet Appliance markets. The VIA C3 processor in EBGA is available in several MHz versions.

When considered individually, the compatibility, function, performance, cost, and power dissipation of the VIA C3 processor family are all very competitive. Furthermore, the value added from the advanced EBGA packaging includes remarkable compactness, cost efficiency and excellent thermal characteristics. The VIA C3 package in EBGA represents a breakthrough combination for enabling high-value, high-performance, low-power, small form factor x86-based solutions. When considered as a whole, the VIA C3 processor family in EBGA offers a peerless level of *value.*

- Enables flexible & innovative system designs
  - Desktop & mobile devices
  - Small, low profile form factors
  - Fanless implementation for ergonomic silent designs
- Optimizes heat dissipation & power consumption
  - Saves energy costs
  - Ensures longer battery life in mobile designs
  - Enhances reliability, particularly for “always on” designs

2.3.2 VIA VT8606 North Bridge

TwisterT (VT8606) is a high performance, cost-effective and energy efficient SMA chip set for the implementation of mobile personal computer systems with 66 MHz, 100 MHz and 133 MHz CPU host bus (“Front Side Bus”) frequencies and based on 64-bit Socket-370 (VIA Cyrix III and Intel Celeron and Tualatin) and Slot-1 (Intel Pentium III) super-scalar processors. TwisterT integrates VIA’s VT82C694T system controller, S3’s Savage4 2D/3D graphics accelerator and S3’s flat panel interfaces into a single 552 BGA package. The TwisterT SMA system controller provides superior performance between the CPU, DRAM and PCI bus with pipelined, burst, and concurrent operation.

TwisterT supports six banks of DRAMs (three memory modules) up to 1.5Gbyte of system memory with 256Mbit DRAM technology. The DRAM controller supports standard Synchronous DRAM (SDRAM) and Virtual Channel SDRAM (VC SDRAM), in a flexible mix / match manner. The Synchronous DRAM interface allows zero wait state bursting between the DRAM and the data buffers at 100 / 133 MHz. The six banks of DRAM can be composed of an arbitrary mixture of 1M / 2M / 4M / 8M / 16M / 32MxN DRAMs. The DRAM controller can run at either the host CPU Front Side Bus frequency (100 / 133 MHz) or pseudo-synchronous to the CPU FSB frequency (PC100 with the FSB at 133 MHz or PC133 with the FSB at 100 MHz) with built-in PLL timing control.

TwisterT supports a 32-bit 3.3 / 5V system bus (PCI) that is synchronous / pseudo-synchronous to the CPU bus. The chip also contains a built-in bus-to-bus bridge to allow simultaneous concurrent operations on each bus. Five levels (doublewords) of post write buffers are included to allow for concurrent CPU and PCI operation. For PCI master operation, forty-eight levels (doublewords) of post write buffers and sixteen levels (doublewords) of prefetch buffers are included for concurrent PCI bus and DRAM/cache accesses. The chip also supports enhanced PCI bus commands such as Memory-Read-Line, Memory-Read-Multiple and Memory-Write-Invalid commands to minimize snoop overhead. In addition, advanced features are supported such as snoop ahead, snoop filtering, L1 write-back forward to PCI master, and L1 write-back merged with PCI post writes buffers to minimize

PCI master read latency and DRAM utilization. Delay transaction and read caching mechanisms are also implemented for further improvement of overall system performance.

TwisterT also integrates S3.'s Savage4 graphics accelerator into a single chip. TwisterT brings mainstream graphics performance to the Value PC with leading-edge 2D, 3D and DVD video acceleration into a cost effective package. Based on its capabilities, TwisterT is an ideal solution for the consumer, corporate mobile users and entry-level professionals.

The industry's first integrated AGP 4X solution, TwisterT combines AGP 4X performance with S3's DX6 texture compression (S3TC) and massive 2Kx2K textures to deliver unprecedented 3D performance and image quality for the Value PC mobile market.

For sophisticated power management, TwisterT provides independent clock stop control for the CPU / SDRAM and PCI and Dynamic CKE control for powering down of the SDRAM. A separate suspend-well plane is implemented for the SDRAM control signals for Suspend-to-DRAM operation.

2.3.2.1 High-Performance 3D Accelerator

Featuring a new super-pipelined 128-bit engine, TwisterT utilizes a single cycle architecture that provides high performance along with superior image quality. Several new features enhance the 3D architecture, including single-pass multitexturing, anisotropic filtering, and an 8-bit stencil buffer. TwisterT also offers the industry's only simultaneous usage of single-pass multitexturing and single-cycle trilinear filtering – enabling stunning image quality without performance loss. TwisterT further enhances image quality with true 32-bit color rendering throughout the 3D pipeline to produce more vivid and realistic images. TwisterT's advanced triangle setup engine provides industry leading 3D performance for a realistic user experience in games and other interactive 3D applications. The 3D engine is optimized for AGP texturing from system memory.

2.3.2.2 128-bit 2D Graphics Engine

TwisterT's advanced 128-bit 2D graphics engine delivers high-speed 2D acceleration for productivity applications. Several enhancements have been made to the 2D architecture to optimize SMA performance and to provide acceleration in all color depths.

2.3.2.3 DVD Playback and Video Conferencing

TwisterT provides the ideal architecture for high quality MPEG-2 based DVD applications and video conferencing. For DVD playback, TwisterT's video accelerator offloads the CPU by performing the planar to packed format conversion and motion compensation tasks, while its enhanced scaling algorithm delivers incredible full-screen video playback. For video conferencing, TwisterT's multiple video windows enable a cost effective solution.

2.3.2.4 LCD and Flat Panel Monitor Support

TwisterT supports a wide variety of DSTN or TFT panels through a 36-bit interface. This includes support for VGA, SVGA, XGA, SXGA+, UXGA, and UXGA+ TFT color panels with 9-bit, 12-bit, 18-bit (both 1 pixel/clock and 2 pixels/clock), and 24-bit interfaces. Enhanced STN hardware with 256 gray scale supports and advanced frame rate control to provide up to 16.7 million colors. In addition, the integrated 2-channel LVDS interface can support another panel. All resolutions are supported up to 1280x1024. The integrated ZV-Port allows display of video from an external source. An alternative to the 36-bit panel interface is a 12-bit interface to a TMDS encoder. This interface is Digital Visual Interface (DVI) 1.0 compliant.

- Defines Integrated Solutions for Value PC Desktops
  - High performance SMA North Bridge: Integrated VIA VT82C694X and S3® Savage4™ 2D/3D graphic accelerator in a single chip
  - 64-bit Advanced Memory controller supporting PC133/PC100 SDRAM
- High Performance CPU Interface
  - Socket 370, Micro-PGA and Micro FCPGA support for Mobile Intel® Pentium™ processors
  - 133/100/66 MHz CPU Front Side Bus (FSB)
  - Built-in Phase Lock Loop circuitry for optimal skew control within and between clocking regions
  - Five outstanding transactions (four In-Order Queue (IOQ) plus one output latch)
  - Dynamic deferred transaction support
- Advanced High - Performance SDRAM Controller
  - DRAM interface runs synchronous (100/100, 133/133) mode or pseudo-synchronous (100/66, 100/133, 133/100) mode with FSB
  - Concurrent CPU, AGP, and PCI access
  - Supports SDRAM and VCM SDRAM memory types
  - Support 3 SODIMMs or 6 banks for up to 1.5 GB of DRAM (256Mb DRAM technology)
  - 64-bit data width
  - Supports maximum 8-bank interleave (8 pages open simultaneously); banks are allocated based on LRU
  - SDRAM X-1-1-1-1-1-1-1 back-to-back accesses

- Integrated Savage4 2D/3D/Video Accelerator
  - Optimized Shared Memory Architecture (SMA)
  - 8/ 16 /32 MB frame buffer using system memory
  - Floating point triangle setup engine
  - Single cycle 128-bit 3D architecture
  - 8M triangles/second setup engine
  - 140M pixels/second trilinear fill rate
  - Full internal AGP 4x performance
  - S3 DX7 texture compression (S3TC™)
  - Next generation, 128-bit 2D graphics engine
  - High quality DVD video playback
  - Flat panel monitor support
  - 2D/3D resolutions up to 1920x1440 for High resolution CRT support,
- 3D Rendering Features
  - Single-pass multiple textures
  - Anisotropic filtering
  - 8-bit stencil buffer
  - 32-bit true color rendering
  - Specular lighting and diffuse shading
  - Alpha blending modes
  - Massive 2K x 2K textures
  - MPEG-2 video textures
  - Vertex and table fog
  - 16 or 24-bit Z-buffering
  - Sprite anti-aliasing, reflection mapping, texture morphing, shadows, procedural textures and atmospheric effects
- 2D Hardware Acceleration Features
  - ROP3 Ternary Raster Operation BitBLTs
  - 8, 16, and 32 bpp mode acceleration
- Motion Video Architecture
  - High quality up/down scaler
  - Planar to packed format conversion
  - Motion compensation for full speed DVD playback
  - Hardware subpicture blending and highlights
  - Multiple video windows for video conferencing
  - Contrast, hue, saturation, brightness and gamma controls
  - Digital port for NTSC/PAL TV encoders

- Extensive LCD Support
  - 36-bit DSTN/TFT flat panel interface with 256 gray shade support
  - Integrated 2-channel 110 MHz LVDS interface
  - Support for all resolutions up to 1280x1024
  - ZV-Port Interface
  - Panel power sequencing
  - Hardware Suspend/Standby control
- Flat Panel Monitor Support
  - 12-bit TFT flat panel interface to TMDS encoders
  - Digital Visual Interface (DVI) 1.0 compliant
- Concurrent PCI Bus Controller
  - PCI 2.2 compliant, 32-bit 3.3V PCI interface with 5V tolerant inputs
  - Supports up to 5 PCI masters
  - PCI to system memory data streaming support
  - Delay transaction from PCI master accessing DRAM
  - Symmetric arbitration between Host/PCI bus for optimized system performance
- Advanced System Power Management Support
  - Dynamic power down of SDRAM (CKE)
  - Independent clock stop controls for CPU / SDRAM, AGP, and PCI bus
  - PCI and AGP bus clock run and clock generator control
  - VTT suspend power plane preserves memory data
  - Suspend-to-DRAM and self-refresh power down
  - Low-leakage I/O pads
  - ACPI 1.0 and PCI Bus Power Management 1.1 compliant

2.3.3 VIA VT82C686B South Bridge

The VT82C686B PSIPC (PCI Super-I/O Integrated Peripheral Controller) is a high integration, high performance, power-efficient, and high compatibility device that supports Intel and non-Intel based processor to PCI bus bridge functionality to make a complete

Microsoft PC99-compliant PCI/ISA system. In addition to complete ISA extension bus functionality, the VT82C686B includes standard intelligent peripheral controllers:

- Master mode enhanced IDE controller with dual channel DMA engine and interlaced dual channel commands. Dedicated FIFO coupled with scatter and gather master mode operation allows high performance transfers between PCI and IDE devices. In addition to standard PIO and DMA mode operation. The VT82C686B also supports the UltraDMA-33, UltraDMA-66, and UltraDMA-100 (ATA-100) standards. The IDE controller is SFF-8038I v1.0 and Microsoft Windows-family compliant.
- Universal Serial Bus controller that is USB v1.1 and Universal HCI v1.1 compliant. The VT82C686B includes the root hub with four function ports with integrated physical layer transceivers. The USB controller allows hot plug and play and isochronous peripherals to be inserted into the system with universal driver support. The controller also implements legacy keyboard and mouse support so that legacy software can run transparently in a non-USB-aware operating system environment.
- Keyboard controller with PS2 mouse support.
- Real Time Clock with 256 byte extended CMOS. In addition to the standard ISA RTC functionality, the integrated RTC also includes the date alarm, century field, and other enhancements for compatibility with the ACPI standard.
- Notebook-class power management functionality compliant with ACPI and legacy APM requirements. Multiple sleep states (power-on suspend, suspend-to-DRAM, and suspend-to-Disk) are supported with hardware automatic wake-up. Additional functionality includes event monitoring, CPU clock throttling and stop (Intel processor protocol), PCI bus clock stop control, modular power, clock and leakage control, hardware-based and software-based event handling, general purpose I/O, chip select and external SMI.
- Hardware monitoring subsystem for managing system / motherboard voltage levels, temperatures, and fan speeds
- Full System Management Bus (SMBus) interface.
- Two 16550-compatible serial I/O ports with infrared communications port option on the second port.

- Integrated PCI-mastering dual full-duplex direct-sound AC97-link-compatible sound system. Hardware soundblaster-pro and hardware-assisted FM blocks are included for Windows DOS box and real-mode DOS compatibility. Loopback capability is also implemented for directing mixed audio streams into USB and 1394 speakers for high quality digital audio.
- Two game ports and one MIDI port
- ECP/EPP-capable parallel port
- Standard floppy disk drive interface
- Distributed DMA capability for support of ISA legacy DMA over the PCI bus. Serial IRQ is also supported for docking and non-docking applications.
- Plug and Play controller that allows complete steerability of all PCI interrupts and internal interrupts / DMA channels to any interrupt channel. One additional steerable interrupt channel is provided to allow plug and play and reconfigurability of on-board peripherals for Windows family compliance.
- Internal I/O APIC (Advanced Programmable Interrupt Controller)

2.3.3.1 IDE Interface (Bus Master Capability and Synchronous DMA Mode)

Master mode enhanced IDE controller with dual channel DMA engine and interlaced dual channel commands. Dedicated FIFO coupled with scatter and gather master mode operation allows high performance transfers between PCI and IDE devices. In addition to standard PIO and DMA mode operation, the VT82C686B also supports the UltraDMA-33, UltraDMA-66, and UltraDMA-100 (ATA-100) standards. The IDE controller is SFF-8038I v1.0 and Microsoft Windows-family compliant.

2.3.3.2 USB

Universal Serial Bus controller is USB v1.1 and Universal HCI v1.1 compliant. The VT82C686B includes the root hub with four function ports with integrated physical layer transceivers. The USB controller allows hot plug and play and isochronous peripherals to be inserted into the system with universal driver support. The controller also implements legacy keyboard and mouse support so that legacy software can run transparently in a non-USB-aware operating system environment.

2.3.4 Realtek RTL8139C Ethernet Controller

The Ethernet interfaces are based on two Realtek RTL8139C Ethernet controllers which support both 100Mbit as well as 10Mbit Base-T interface.

The Ethernet controllers are attached to the PCI bus and use PCI bus mastering for data transfer. The CPU is thereby not loaded during the actual data transfer.

The Realtek RTL8139C is a highly integrated and cost-effective single-chip Fast Ethernet controller that provides 32-bit performance, PCI bus master capability, and full compliance with IEEE 802.3u 100Base-T specifications and IEEE 802.3x Full Duplex Flow Control. It also supports Advanced Configuration Power management Interface (ACPI), PCI power management for modern operating systems that is capable of Operating System Directed Power Management (OSPM) to achieve the most efficient power management.

2.3.5 Intel 82559ER Ethernet Controller (Optional)

The 82559ER is part of Intel's second-generation family of fully integrated 10BASE-T/100BASE-TX LAN solutions. The 82559ER consists of both the Media Access Controller (MAC) and the physical layer (PHY) combined into a single component solution. 82559 family members build on the basic functionality of the 82558 and contain power management enhancements.

The 82559ER is a 32-bit PCI controller that features enhanced scatter-gather bus mastering capabilities enables the 82559ER to perform high-speed data transfers over the PCI bus. The 82559ER bus master capabilities enable the component to process high-level commands and perform multiple operations, thereby off-loading communication tasks from the system CPU. Two large transmit and receive FIFOs of 3 Kbytes each help prevent data underruns and overruns, allowing the 82559ER to transmit data with minimum interframe spacing (IFS).

The 82559ER can operate in either full duplex or half duplex mode. In full duplex mode the 82559ER adheres to the IEEE 802.3x Flow Control specification. Half duplex performance is enhanced by a proprietary collision reduction mechanism.

The 82559ER includes a simple PHY interface to the wire transformer at rates of 10BASE-T and 100BASE-TX, and Auto-Negotiation capability for speed, duplex, and flow control. These features and others reduce cost, real estate, and design complexity.

The 82559ER also includes an interface to a serial (4-pin) EEPROM and a parallel interface to a 128 Kbytes Flash memory. The EEPROM provides power-on initialization for hardware and software configuration parameters

2.3.6 VIA VT6306 IEEE1394A Host Controller

The VT6306 IEEE 1394 OHCI Host Controller provides high performance serial connectivity. It implements the Link and Phy layers for IEEE 1394-1995 High Performance Serial Bus and 1394a Draft 4.0. It is compliant with 1394 Open HCI 1.0 and 1.1 with DMA engine support for high performance data transfer via a 32-bit bus master PCI host bus interface.

The VT6306 supports 100, 200 and 400 Mbit/sec transmissions via an integrated 3-port PHY. The VT6306 services two types of data packets: asynchronous and isochronous (real time). The 1394 link core performs arbitration requesting, packet generation and checking, and bus cycle master operations. It also has root node capability and performs retry operations.

The VT6306 is ready to provide industry-standard IEEE 1394 peripheral connections for desktop and mobile PC platforms. Support for the VT6306 is built into Microsoft Windows 98, Windows ME, and Windows 2000.

2.3.7 VIA VT1621 Digital TV Encoder

VT1621 is a digital television encoder that accepts video pixel data stream from a VGA controller or MPEG decoder and produces NTSC or PAL (B, D, G, H, I) TV format directly. VT1621 incorporates serial bus host interface that provides read/write access to all programmable registers. The input video is compliant with CCIR656. IT supports SVideo, Compose video and SCART outputs. It can accept input video data resolution format from 320 x 200 up to 800 x 600. Welkin's VT1621 incorporates Welkin's ProScale engine to eliminate flicker when display the non-interlaced video data to interlaced devices. This Proscale engine also converts the lines of input video stream data to the appropriate number of output lines for producing a high quality TV image.

2.3.8 Compact Flash Interface

A Compact Flash type II connector is connected to the secondary IDE controller. The Compact Flash storage card is IDE compatible. It is an ideal replacement for standard IDE hard drives. The solid-state design offers no seek errors even under extreme shock and vibration conditions. The Compact Flash storage card is extremely small and highly suitable for rugged environments, thus providing an excellent solution for mobile applications with space limitations. It is fully compatible with all consumer applications designed for data storage PC card, PDA, and Smart Cellular Phones, allowing simple use for the end user. The Compact Flash storage card is O/S independent, thus offering an optimal solution for embedded systems operating in non-standard computing environments. The Compact Flash storage card is IDE compatible and offers various capacities.

3. Hardware Configuration

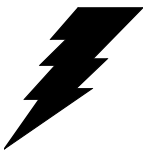
This chapter explains you the instructions of how to setup your system.

3.1 Installation Procedure

1. Turn off the power supply.
2. Insert the DIMM module (be careful with the orientation).
3. Insert all external cables for hard disk, floppy, keyboard, mouse, USB etc. except for flat panel. A CRT monitor must be connected in order to change CMOS settings to support flat panel.
4. Connect power supply to the board via the PWR1.
5. Turn on the power.
6. Enter the BIOS setup by pressing the delete key during boot up. Use the "LOAD BIOS DEFAULTS" feature. The ***Integrated Peripheral Setup*** and the ***Standard CMOS Setup*** Window must be entered and configured correctly to match the particular system configuration.
7. If TFT panel display is to be utilised, make sure the panel voltage is correctly set before connecting the display cable and turning on the power.

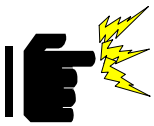
3.2 Safety Precautions

3.2.1 Warning!



Always completely disconnect the power cord from your chassis or power cable from your board whenever you work with the hardware. Do not make connections while the power is on. Sensitive electronic components can be damaged by sudden power surges. Only experienced electronics personnel should open the PC chassis.

3.2.2 Caution!



Always ground yourself to remove any static charge before touching the board. Modern electronic devices are very sensitive to static electric charges. As a safety precaution, use a grounding wrist strap at all times. Place all electronic components in a static-dissipative surface or static-shielded bag when they are not in the chassis.

3.3 Socket 370 Processor (EBC-5612 Series Only)

3.3.1 Installing Pentium III / Celeron CPU

- Lift the handling lever of CPU socket outwards and upwards to the other end.
- Align the processor pins with pinholes on the socket. Make sure that the notched corner or dot mark (pin 1) of the CPU corresponds to the socket's bevel end. Then press the CPU gently until it fits into place. If this operation is not easy or smooth, don't do it forcibly. You need to check and rebuild the CPU pin uniformly.
- Push down the lever to lock processor chip into the socket.
- Follow the installation guide of cooling fan or heat sink to mount it on CPU surface and lock it on the socket 370.
- Make sure to follow particular CPU speed and voltage type to adjust the jumper settings properly.

3.3.2 Removing CPU

- Unlock the cooling fan first.
- Lift the lever of CPU socket outwards and upwards to the other end.
- Carefully lift up the existing CPU to remove it from the socket.
- Follow the steps of installing a CPU to change to another one or place handling bar back to close the opened socket.

3.4 Main Memory

EBC5612 provides a DIMM socket (168-pin Dual In-line Memory Module) to support 3.3V SDRAM. The maximum memory size is 256MB (registered type of SDRAM). If 133MHz FSB CPU is adopt, you have to use PC-133 compliant SDRAM. For system compatibility and stability, please do not use memory module without brand.

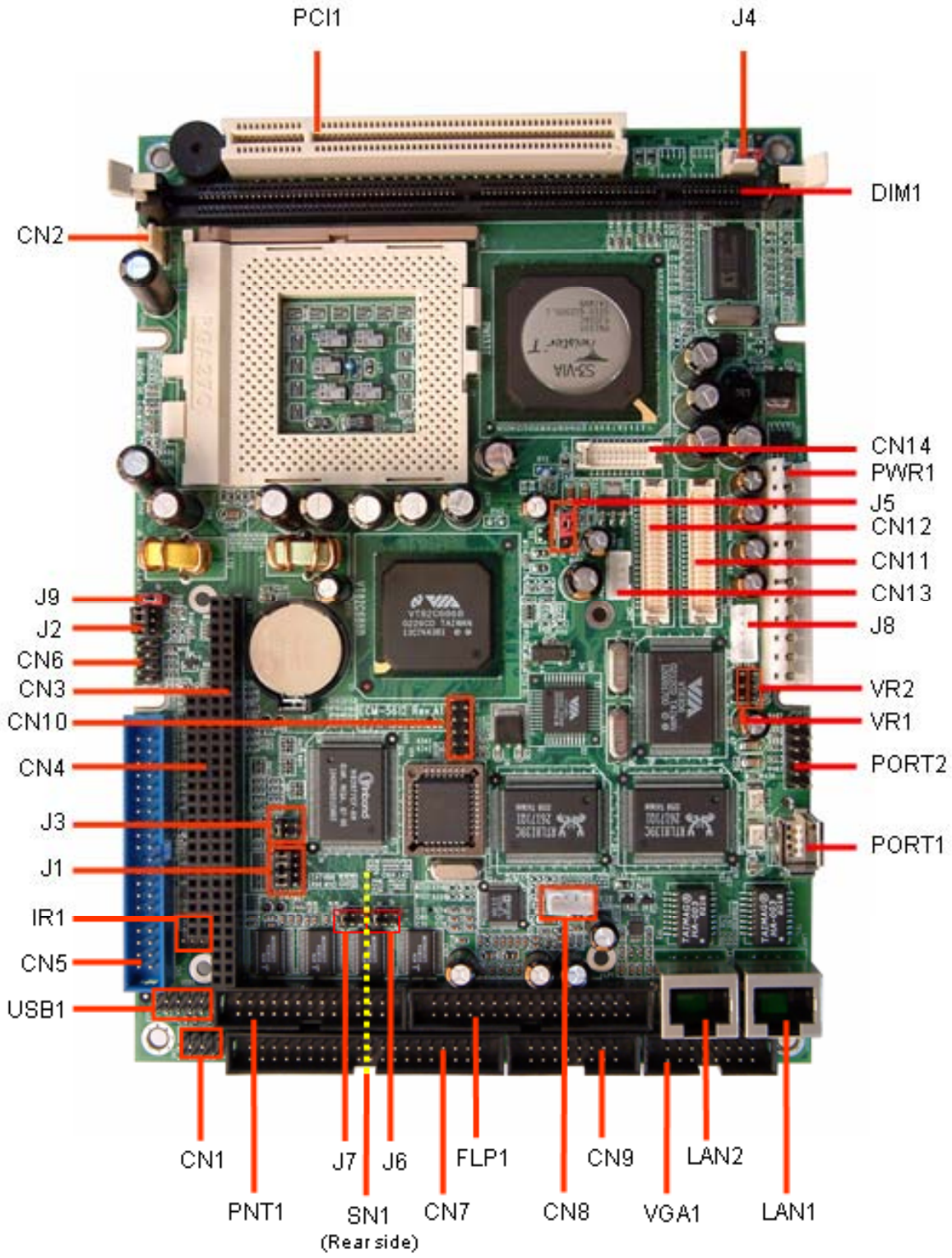
Watch out the contact and lock integrity of memory module with socket, it will influence the system's reliability. Follow the normal procedure to install your SDRAM module into the DIMM socket. Before locking the DIMM module, make sure that the memory module has been completely inserted into the DIMM socket.

Note:

Please do not change any SDRAM parameter in BIOS setup to increase your system's performance without acquiring technical information in advance.

3.5 Jumper & Connector

3.5.1 Jumper & Connector Layout



3.5.2 Jumper & Connector List

Connectors on the board are linked to external devices such as hard disk drives, keyboard, mouse, or floppy drives. In addition, the board has a number of jumpers that allow you to configure your system to suit your application.

The following tables list the function of each of the board's jumpers and connectors.

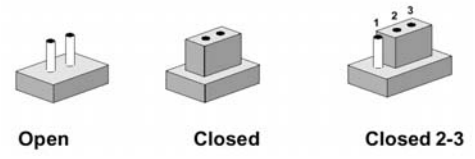
Jumpers		
Label	**Function**	**Note**
J1, J3	COM2 RS-232/422/485 select	4 x 3 header, pitch 2.0mm (J1) 3 x 2 header, pitch 2.0mm (J3)
J5	Clear CMOS	3 x 1 header, pitch 2.54mm
J6	COM3 pin 9 signal select	3 x 2 header, pitch 2.0mm
J7	COM4 pin 9 signal select	3 x 2 header, pitch 2.0mm
J9	AT / ATX power select	3 x 1 header, pitch 2.0mm

Connectors		
Label	**Function**	**Note**
CN1	Keyboard and PS/2 mouse connector	4 x 2 header, pitch 2.54mm
CN2	CPU fan connector	3 x 1 wafer, pitch 2.54mm
CN3, 4	PC/104 connector	
CN5	IDE device connector	20 x 2 header, pitch 2.54mm
CN6	Front panel connector	4 x 2 header, pitch 2.54mm
CN7	Serial port 1 / 2 / 3 / 4 connector	20 x 2 header, pitch 2.54mm
CN8	CD-ROM audio input connector	4 x 1 wafer, pitch 2.0mm
CN9	Audio / TV output connector	8 x 2 header, pitch 2.54mm
CN10	Ethernet 1 / 2 LED connector	5 x 2 header, pitch 2.54mm
CN11	Primary LCD panel connector	HIROSE DF13-40DP-1.25V
CN12	Secondary LCD panel connector	HIROSE DF13-40DP-1.25V
CN14	Zoom Video port connector	HIROSE DF13-20DP-1.25V
FLP1	Floppy connector	17 x 2 header, pitch 2.54mm
IR1	IrDA connector	3 x 2 header, pitch 2.0mm
J4	Power connector	3 x 1 wafer, pitch 2.54mm
J8	LCD inverter connector	5 x 1 wafer, pitch 2.0mm
LAN1	10/100Base-Tx Ethernet 1 connector	RJ-45
LAN2	10/100Base-Tx Ethernet 2 connector	RJ-45
PCI1	PCI connector	
PNT1	Printer port connector	13 x 2 header, pitch 2.54mm
PORT1	IEEE1394 port 1 connector	
PORT2	IEEE 1394 port 2/3 connector	6 x 2 header, pitch 2.54mm
PWR1	Power connector	AT power connector
SN1	Compact Flash connector	
USB1	USB connector	5 x 2 header, pitch 2.54mm
VGA1	CRT connector	8 x 2 header, pitch 2.54mm
VR1	STN LCD contrast adjustment connector	3 x 1 header, pitch 2.54mm
VR2	LCD Backlight brightness adjustment connector	3 x 1 header, pitch 2.54mm
DIM1	168-pin DIMM socket	

3.6 Setting Jumpers

You can configure your board to match the needs of your application by setting jumpers. A jumper is the simplest kind of electric switch.

It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To “close” a jumper you connect the pins with the clip. To “open” a jumper you remove the clip. Sometimes a jumper will have three pins, labeled 1, 2, and 3. In this case, you would connect either two pins.



The jumper settings are schematically depicted in this manual as follows:

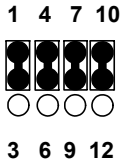
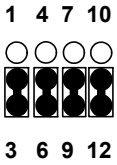
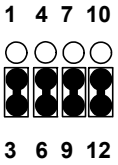
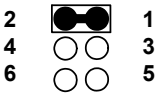
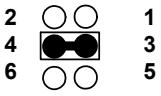
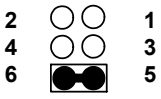
A pair of needle-nose pliers may be helpful when working with jumpers.

If you have any doubts about the best hardware configuration for your application, contact your local distributor or sales representative before you make any changes.

3.6.1 COM2 RS-232/422/485 Select (J1, J3)

The EBC5612 COM2 serial port can be selected as RS-232, RS-422, or RS-485 by setting J1 & J3.

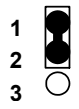
COM2 RS/232/422/485 Select (J1, J3)

	RS-232*	RS-422	RS-485
J1			
J3			

* default

3.6.2 Clear CMOS (J5)

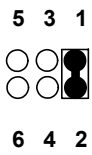
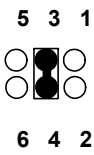
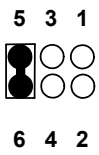
You can use J5 to clear the CMOS data if necessary. To reset the CMOS data, set J5 to 2-3 closed for just a few seconds, and then move the jumper back to 1-2 closed.

Clear CMOS (J5)		
	Protect*	Clear CMOS
J5		

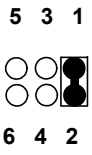
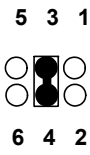
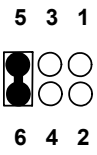
* default

3.6.3 COM3 / 4 Pin 9 Signal Select (J6 / J7)

The EBC5612 COM3 / 4 pin 9 signal can be selected as +12V, +5V, or Ring by setting J6 / J7.

COM3 Pin 9 Signal Select (J6)			
	+12V	+5V	Ring*
J6			

* default

COM4 Pin 9 Signal Select (J7)			
	+12V	+5V	Ring*
J7			

* default

3.6.4 AT/ATX Power Select (J9)

You can use J9 to select the power supply type. Using AT power supply, set J9 to 1-2 closed. Set J9 to 2-3 closed, if ATX power supply is to be used.

AT/ATX Power Select (J9)		
	AT P/S*	ATX P/S
J9		

* default

Note:

Set J4 to 2-3 closed. If AT power supply is to be used.

3.7 Connector Definitions

3.7.1 Keyboard and PS/2 Mouse Connector (CN1)

Signal	PIN		Signal
KDAT	1	5	KDAT
GND	2	6	GND
MDAT	3	7	MDAT
NC	4		NC

3.7.2 Signal Description – Keyboard / Mouse Connector (CN1)

KCLK	Bi-directional clock signal used to strobe data/commands from/to the PC-AT keyboard.
KDAT	Bi-directional serial data line used to transfer data from or commands to the PC-AT keyboard.
MCLK	Bi-directional clock signal used to strobe data/commands from/to the PS/2 mouse.
MDAT	Bi-directional serial data line used to transfer data from or commands to the PS/2 mouse.

3.7.3 CPU Fan Connector (CN2)

Signal	PIN
TAC	3
+12V	2
GND	1

3.7.4 Signal Description – CPU Fan Connector (CN2)

TAC	Fan speed monitor

3.7.5 PC/104 Connector (CN3, CN4)

Signal	PIN		PIN		Signal
GND	B32	A32			GND
GND	B31	A31			SA0
OSC	B30	A30			SA1
VCC	B29	A29			SA2
BALE	B28	A28			SA3
NC			C19	D19	GND
TC	B27	A27			SA4
SD15			C18	D18	GND
DACK2#	B26	A26			SA5
SD14			C17	D17	MASTER#
IRQ3	B25	A25			SA6
SD13			C16	D16	VCC
IRQ4	B24	A24			SA7
SD12			C15	D15	DRQ7
IRQ5	B23	A23			SA8
SD11			C14	D14	DACK7#
IRQ6	B22	A22			SA9
SD10			C13	D13	DRQ6
IRQ7	B21	A21			SA10
SD9			C12	D12	DACK6#
SYSCLK	B20	A20			SA11
SD8			C11	D11	DRQ5
REFRESH#	B19	A19			SA12
SMEMW#			C10	D10	DACK5#
DRQ1	B18	A18			SA13
SMEMR#			C9	D9	DRQ0
DACK1#	B17	A17			SA14
LA17			C8	D8	DACK0#
DRQ3	B16	A16			SA15
LA18			C7	D7	IRQ14
DACK3#	B15	A15			SA16
LA19			C6	D6	IRQ15
IOR#	B14	A14			SA17
LA20			C5	D5	IRQ12
IOW#	B13	A13			SA18
LA21			C4	D4	IRQ11
SMEMR#	B12	A12			SA19
LA22			C3	D3	IRQ10
SMEMW#	B11	A11			AEN
LA23			C2	D2	IOCS16#
GND	B10	A10			IOCHRDY
SBHE#			C1	D1	MEMCS16#
+ 12 V	B9	A9			SD0
GND			C0	D0	GND
OWS#	B8	A8			SD1
- 12 V	B7	A7			SD2
DRQ2	B6	A6			SD3
- 5 V	B5	A5			SD4
IRQ9	B4	A4			SD5
VCC	B3	A3			SD6
RESETDRV	B2	A2			SD7
GND	B1	A1			IOCHCHK#

3.7.6 Signal Description – PC/104 Connector (CN3, CN4)

3.7.6.1 Address

LA [23:17]	The address signals LA [23:17] define the selection of a 128KB section of memory space within the 16MB address range of the 16-bit data bus. These signals are active high. The validity of the MEMCS16# depends on these signals only. These address lines are presented to the system with tri-state drivers. The permanent master drives these lines except when an alternate master cycle occurs; in this case, the temporary master drives these lines. The LA signals are not defined for I/O accesses.
SA [19:0]	System address. Address lines for the first one Megabyte of memory. SA [9:0] used for I/O addresses. SA0 is the least significant bit
SBHE#	This signal is an active low signal, that indicates that a byte is being transferred on the upper byte (SD [15:8]) of the 16 bit bus. All bus masters will drive this line with a tri-state driver.

3.7.6.2 Data

SD [15:8]	These signals are defined for the high order byte of the 16-bit data bus. Memory or I/O transfers on this part of the bus are defined when SBHE# is active.
SD [7:0]	These signals are defined for the low order byte of the 16-bit data bus being the only bus for 8 bit PC-AT/PC104 adapter boards. Memory or I/O transfers on this part of the data bus are defined for 8-bit operations with even or odd addresses and for 16-bit operations for odd addresses only. The signals SA0 and SBHE# are used to define the data present on this bus:

SBHE#	SA0	SD15-SD8	SD7-SD0	Action
0	0	ODD	EVEN	Word transfer
0	1	ODD	ODD	Byte transfer on SD15-SD8
1	0	-	EVEN	Byte transfer on SD7-SD0
1	1	-	ODD	Byte transfer on SD7-SD0

3.7.6.3 Commands

BALE	This is an active high signal used to latch valid addresses from the current bus master on the falling edge of BALE. During DMA, refresh and alternate master cycles, BALE is forced high for the duration of the transfer. BALE is driven by the permanent master with a totem-pole driver.
IOR#	This is an active low signal driven by the current master to indicate an I/O read operation. I/O mapped devices using this strobe for selection should decode addresses SA [15:0] and AEN. Additionally, DMA devices will use IOR# in conjunction with $DACK_n$# to decode a DMA transfer from the I/O device. The current bus master will drive this line with a tri-state driver.
IOW#	This is an active low signal driven by the current master to indicate an I/O write operation. I/O mapped devices using this strobe for selection should decode addresses SA [15:0] and AEN. Additionally, DMA devices will use IOR# in conjunction with $DACK_n$# to decode a DMA transfer from the I/O device. The current bus master will drive this line with a tri-state driver.
SMEMR#	This is an active low signal driven by the permanent master to indicate a memory read operation in the first 1MB of system memory. Memory mapped devices using this strobe should decode addresses SA [19:0] only. If an alternate master drives MEMR#, the permanent master will drive SMEMR# delayed by internal logic. The permanent master ties this line to VCC through a pull-up resistor to ensure that it is inactive during the exchange of bus masters.
SMEMW#	This is an active low signal driven by the permanent master to indicate a memory write operation in the first 1MB of system memory. Memory mapped devices using this strobe should decode addresses SA [19:0] only. If an alternate master drives MEMR#, the permanent master will drive SMEMR# delayed by internal logic. The permanent master ties this line to VCC through a pull-up resistor to ensure that it is inactive during the exchange of bus masters.
MEMR#	This is an active low signal driven by the current master to indicate a memory read operation. Memory mapped devices using this strobe should decode addresses LA [23:17] and SA [19:0]. All bus masters will drive this line with a tri-state driver. The permanent master ties this line to VCC through a pull-up resistor to ensure that it is inactive during the exchange of bus masters.
MEMW#	This is an active low signal driven by the current master to indicate a memory write operation. Memory mapped devices using this strobe should decode addresses LA [23:17] and SA [19:0]. All bus masters will drive this line with a tri-state driver. The permanent master ties this line to VCC through a pull-up resistor to ensure that it is inactive during the exchange of bus masters.

3.7.6.4 Transfer Response

IOCS16#	This is an active low signal driven by an I/O-mapped PC-AT/PC104 adapter indicating that the I/O device located at the address is a 16-bit device. This open collector signal is driven, based on SA [15:0] only (not IOR# and IOW#) when AEN is not asserted.
MEMCS16#	This is an active low signal driven by a memory mapped PC-AT/PC104 adapter indicating that the memory device located at the address is a 16-bit device. This open collector signal is driven, based on LA [23:17] only.
0WS#	This signal is an active low open-collector signal asserted by a 16-bit memory mapped device that may cause an early termination of the current transfer. It should be gated with MEMR# or MEMW# and is not valid during DMA transfers. IOCHRDY precedes 0WS#.
IOCHRDY	This is an active high signal driven inactive by the target of either a memory or an I/O operation to extend the current cycle. This open collector signal is driven based on the system address and the appropriate control strobe. IOCHRDY precedes 0WS#.
IOCHCK#	This is an active low signal driven active by a PC-AT/PC104 adapter detecting a fatal error during bus operation. When this open collector signal is driven low it will typically cause a non-maskable interrupt.

3.7.6.5 Controls

SYSCLK	This clock signal may vary in frequency from 2.5 MHz to 25.0 MHz depending on the setup made in the BIOS. Frequencies above 16 MHz are not recommended. The standard states 6 MHz to 8.33 MHz, but most new adapters are able to handle higher frequencies. The PC-AT/PC104 bus timing is based on this clock signal.
OSC	This is a clock signal with a 14.31818 MHz ± 50 ppm frequency and a 50 ± 5% duty cycle. The signal is driven by the permanent master.
RESETDRV	This active high signal indicates that the adapter should be brought to an initial reset condition. This signal will be asserted by the permanent master on the bus for at least 100 ms at power-up or watchdog time-out to ensure that adapters in the system are properly reset. When active, all adapters should turn off or tri-state all drivers connected to the bus.

3.7.6.6 Interrupts

IRQ [3:7], IRQ [9:12], IRQ [14:15]	These signals are active high signals, which indicate the presence of an interrupting PC-AT/PC104 bus adapter. Due to the use of pull-ups, unused interrupt inputs must be masked.

3.7.6.7 Bus Arbitration

DRQ [0:3], DRQ [5:7]	These signals are active high signals driven by a DMA bus adapter to indicate a request for a DMA bus operation. DRQ [0:3] request 8 bit DMA operations, while DRQ [5:7] request 16 bit operations. All bus DMA adapters will drive these lines with a tri-state driver. The permanent master monitors these signals to determine which of the DMA devices, if any, are requesting the bus.
DACK [0:3]#, DACK [5:7]#	These signals are active low signals driven by the permanent master to indicate that a DMA operation can begin. They are continuously driven by a totem pole driver for DMA channels attached.
AEN	This signal is an active high totem pole signal driven by the permanent master to indicate that the address lines are driven by the DMA controller. The assertion of AEN disables response to I/O port addresses when I/O command strobes are asserted. AEN being asserted, only the device with active $DACK_n$# should respond.
REFRESH#	This is an active low signal driven by the current master to indicate a memory refresh operation. The current master will drive this line with a tri-state driver.
TC	This active high signal is asserted during a read or write command indicating that the DMA controller has reached a terminal count for the current transfer. $DACK_n$# must be presented by the bus adapter to validate the TC signal.
MASTER#	This signal is not supported by the chipset.

3.7.7 IDE Device Connector (CN5)

Signal	PIN		Signal
GND	40	39	DACT#
DCS3#	38	37	DCS1#
DA2	36	35	DA0
NC	34	33	DA1
NC	32	31	IRQ14
GND	30	29	DACK#
GND	28	27	IORDY
GND	26	25	IOR#
GND	24	23	IOW#
GND	22	21	DREQ
NC	20	19	GND
D15	18	17	D0
D14	16	15	D1
D13	14	13	D2
D12	12	11	D3
D11	10	9	D4
D10	8	7	D5
D9	6	5	D6
D8	4	3	D7
GND	2	1	RESET#

3.7.8 Signal Description – IDE Device Connector (CN5)

The IDE interface supports PIO modes 0 to 4 and Bus Master IDE. Data transfer rates up to 100 MB/Sec is possible.

DA [2:0]	IDE Address Bits. These address bits are used to access a register or data port in a device on the IDE bus.
DCS1#, DCS3#	IDE Chip Selects. The chip select signals are used to select the command block registers in an IDE device. DCS1# selects the primary hard disk.
D [15:0]	IDE Data Lines. D [15:0] transfers data to/from the IDE devices.
IOR#	IDE I/O Read. Signal is asserted on read accesses to the corresponding IDE port addresses.
IOW#	IDE I/O Write. Each signal is asserted on write accesses to corresponding the IDE port addresses.
IORDY	When deasserted, these signals extend the transfer cycle of any host register access when the device is not ready to respond to the data transfer request.
RESET#	IDE Reset. This signal resets all the devices that are attached to the IDE interface.
IRQ14	Interrupt line from hard disk. Connected directly to PC-AT bus.
DREQ	The DREQ is used to request a DMA transfer from the South Bridge. The direction of the transfers is determined by the IOR#/IOW# signals.
DACK#	DMA Acknowledge. The DACK# acknowledges the DREQ request to initiate DMA transfers.
DACT#	Signal from hard disk indicating hard disk activity. The signal level depends on the hard disk type, normally active low. The signal is routed directly to the LED1.

3.7.9 Front Panel Connector (CN6)

Signal	PIN		Signal
HD_LED	1	5	VCC
GND	2	6	SPK
PWBTI	3	7	GND
RSTIN	4	8	GND

3.7.10 Signal Description – Front Panel Connector (CN6)

HD_LED	IDE device activity signal
PWBTI	Power Button
RSTIN	System Reset
SPK	External Speaker

3.7.11 Pin Header Serial Port 1 / 2 / 3 / 4 Connector in RS-232 Mode (CN7)

Signal	PIN		Signal
DCD1	1	2	DSR1
RxD1	3	4	RTS1
TxD1	5	6	CTS1
DTR1	7	8	RI1
GND	9	10	NC
DCD2	11	12	DSR2
RxD2	13	14	RTS2
TxD2	15	16	CTS2
DTR2	17	18	RI2
GND	19	20	NC
DCD3	21	22	DSR3
RxD3	23	24	RTS3
TxD3	25	26	CTS3
DTR3	27	28	RI3/5V/12V
GND	29	30	NC
DCD4	31	32	DSR4
RxD4	33	34	RTS4
TxD4	35	36	CTS4
DTR4	37	38	RI4/5V/12V
GND	39	40	NC

3.7.12 Serial Port 1 / 2 / 3 / 4 with External DB9 Connector (CN7)

Signal	PIN		Signal
GND	5		
		9	RI
DTR	4		
		8	CTS
TxD	3		
		7	RTS
RxD	2		
		6	DSR
DCD	1		

3.7.13 Signal Description – Serial Port 1 / 2 / 3 / 4 Connector in RS-232 Mode (CN7)

TxD	Serial output. This signal sends serial data to the communication link. The signal is set to a marking state on hardware reset when the transmitter is empty or when loop mode operation is initiated.
RxD	Serial input. This signal receives serial data from the communication link.
DTR	Data Terminal Ready. This signal indicates to the modem or data set that the on-board UART is ready to establish a communication link.
DSR	Data Set Ready. This signal indicates that the modem or data set is ready to establish a communication link.
RTS	Request To Send. This signal indicates to the modem or data set that the on-board UART is ready to exchange data.
CTS	Clear To Send. This signal indicates that the modem or data set is ready to exchange data.
DCD	Data Carrier Detect. This signal indicates that the modem or data set has detected the data carrier.
RI	Ring Indicator. This signal indicates that the modem has received a telephone ringing signal.

3.7.14 Pin Header Serial Port 2 Connector in RS-422 Mode (CN7 / Pin 11~20)

Signal	PIN		Signal
Tx-	11	12	NC
Rx+	13	14	NC
Tx+	15	16	NC
Rx-	17	18	NC
GND	19	20	NC

3.7.15 Signal Description – Serial Port 2 in RS-422 Mode (CN7 / Pin 11~20)

Tx +/-	Serial output. This differential signal pair sends serial data to the communication link. Data is transferred from Serial Port 2 Transmit Buffer Register to the communication link, if the RTS register of the Serial Port 2 is set to LOW.
Rx +/-	Serial input. This differential signal pair receives serial data from the communication link. Received data is available in Serial Port 2 Receiver Buffer Register.

3.7.16 Pin Header Serial Port 2 Connector in RS-485 Mode (CN7 / Pin 11~20)

Signal	PIN		Signal
DATA-	11	12	NC
NC	13	14	NC
DATA+	15	16	NC
NC	17	18	NC
GND	19	20	NC

3.7.17 Signal Description – Serial Port 2 in RS-485 Mode (CN7 / Pin 11~20)

DATA +/-	This differential signal pair sends and receives serial data to the communication link. The mode of this differential signal pair is controlled through the RTS register of Serial Port 2. Set the RTS register of the Serial Port 2 to LOW for transmitting, HIGH for receiving.

Warning: Do not select a mode different from the one used by the connected peripheral, as this may damage CPU board and/or peripheral.

The transmitter drivers in the port are short circuit protected by a thermal protection circuit. The circuit disables the drivers when the die temperatures reach 150 °C.

RS-422 mode is typically used in point to point communication. Data and control signal pairs should be terminated in the receiver end with a resistor matching the cable impedance (typ. 100-120 Ω). The resistors could be placed in the connector housing.

RS-485 mode is typically used in multi drop applications, where more than 2 units are communicating. The data and control signal pairs should be terminated in each end of the communication line with a resistor matching the cable impedance (typical 100-120 Ω). Stubs to substations should be avoided.

3.7.18 CD-ROM Audio Input Connector (CN8)

Signal	PIN
CD_GND	1
CD_L	2
CD_GND	3
CD_R	4

3.7.19 Signal Description – CD-ROM Input Connector (CN8)

CD L/R	Left and right CD audio input lines.
CD_GND	GND for left and right CD. This GND level is not connected to the board GND.

3.7.20 Audio / TV Output Connector (CN9)

Signal	PIN		Signal
Mic	1	2	Mic Bias
AGND	3	4	AGND
Line-Out L	5	6	Line-Out R
SPK L	7	8	SPK R
Line-In L	9	10	Line-In R
AGND	11	12	Yout
GND	13	14	Cout
GND	15	16	COMP

3.7.21 Signal Description – Audio / TV Output Connector (CN9)

SPK L/R	Left and right speaker output. These are the speaker outputs directly from the speaker amplifier. Coupling capacitors must be used in order to avoid DC-currents in the speakers. If the Audio Bracket is used these signals are supplied on the PCB. GND should be used as return for each speaker. Maximum power: 0.5W@4 Ω load for each channel.
Mic / Mic Bias	The MIC signal is used for microphone input. This input is fed to the left microphone channel. Mic Bias provides 3.3V supplied through 3.2K Ω with capacitive decoupling to GND. This signal may be used for bias of some microphone types.
Line-In L/R	Left and right line in signals.
Line-Out L/R	Left and right line out signals. Both signals are capacitor coupled and should have GND as return.
Yout	Luminance output
Cout	Chrominance output
COMP	Composit video output

3.7.22 Ethernet 1 / 2 LED Connector (CN10)

Signal	PIN		Signal
SPDLED1	10	9	SPDLED2
GND	8	7	VCC3SB
LINKLED1	6	5	LINKLED2
ACTLED1	4	3	ACTLED2
VCCS3B	2	1	GND

3.7.23 Signal Description – Ethernet 1 / 2 LED Connector (CN10)

ACTLED1# / 2#	Activity LED. The Activity LED pin indicates either transmits or receives activity. When activity is present, the activity LED is on; when no activity is present, the activity LED is off. Work with VCC3SB.
LILED1# / 2#	Link Integrity LED. The Link Integrity LED pin indicates link integrity. If the link is valid in either 10 or 100 Mbps, the LED is on; if link is invalid, the LED is off. Work with VCC3SB.
SPDLED1# / 2#	Speed LED. The Speed LED pin indicates the speed. The speed LED will be on at 100 Mbps and off at 10 Mbps. Work with VCC3SB.

3.7.23.1 Primary LCD Panel Connector (CN11)

Signal	PIN		Signal
5V	2	1	5V
GND	4	3	GND
3.3V	6	5	3.3V
GND	8	7	Vcon
P1	10	9	P0
P3	12	11	P2
P5	14	13	P4
P7	16	15	P6
P9	18	17	P8
P11	20	19	P10
P13	22	21	P12
P15	24	23	P14
P17	26	25	P16
P19	28	27	P18
P21	30	29	P20
P23	32	31	P22
GND	34	33	GND
FLM	36	35	SHFCLK
LP	38	37	M
ENVEE	40	39	ENBKL

3.7.24 Secondary LCD Panel Connector (CN12)

Signal	PIN		Signal
5V	2	1	5V
GND	4	3	GND
3.3V	6	5	3.3V
GND	8	7	Vcon
P25	10	9	P24
P27	12	11	P26
P29	14	13	P28
P31	16	15	P30
P33	18	17	P32
P35	20	19	P34
GND	22	21	GND
Y2M	24	23	Y2P
Z1M	26	25	Z1P
ZCM	28	27	ZCP
Z0M	30	29	Z0P
YCM	32	31	YCP
GND	34	33	GND
Y0M	36	35	Y0P
Z2M	38	37	Z2P
Y1M	40	39	Y1P

3.7.25 Signal Description – Primary & Secondary LCD Panel Connector (CN11, CN12)

P [35:0]	Flat Panel Data Bit 35 to Bit 0 for panel implementation.
SHFCLK	Shift Clock. Pixel clock for flat panel data
LP	Latch Pulse. Flat panel equivalent of HSYNC (horizontal synchronization)
FLM	First Line Marker. Flat panel equivalent of VSYNC (vertical synchronization)
M	Multipurpose signal, function depends on panel type. May be used as AC drive control signal or as BLANK# or Display Enable signal
ENBKL	Enable backlight signal. This signal is controlled as a part of the panel power sequencing
ENVEE	Enable VEE. Signal to control the panel power-on/off sequencing. A high level may turn on the VEE (LCD bias voltage) supply to the panel
Y[2:0]P, Z[2:0]P	1st & 2nd Channel Positive LVDS differential data output
Y[2:0]M, Z[2:0]M	1st & 2nd Channel Negative LVDS differential data output
YCP, ZCP	1st & 2nd Channel Positive LVDS differential clock output
YCM, ZCM	1st & 2nd Channel Negative LVDS differential clock output

3.7.26 Signal Configuration – DSTN Displays

	STN			DSTN				
Pin name	8-bit	16-bit	24-bit	8-bit	16-bit	24-bit	16-bit	24-bit
P35								
P34								
P33								
P32					UG2	UG2		
P31								
P30					UR2	UR2		
P29						UB3		
P28					UB1	UB1		
P27								
P26					UG1	UG1		
P25						UG3		
P24				UR1	UR1	UR1		
P23			B7				UR0	UR0
P22			G7	UB0	UB0	UB0	UR1	UR1
P21			R7				UR2	UR2
P20			B6	UG0	UG0	UG0		UR3
P19			G6			UR3	LR0	LR0
P18			R6	UR0	UR0	UR0	LR1	LR1
P17			B5				LR2	LR2
P16			G5					LR3
P15		R5	R5				UG0	UG0
P14		B4	B4		LG2	LG2	UG1	UG1
P13		G4	G4			LB3	UG2	UG2
P12		R4	R4		LR2	LR2		UG3
P11		B3	B3				LG0	LG0
P10		G3	G3		LB1	LB1	LG1	LG1
P9		R3	R3				LG2	LG2
P8		B2	B2		LG1	LG1		LG3
P7	G2	G2	G2			LG3	UB0	UB0
P6	R2	R2	R2	LR1	LR1	LR1	UB1	UB1
P5	B1	B1	B1					UB2
P4	G1	G1	G1	LB0	LB0	LB0		UB3
P3	R1	R1	R1				LB0	LB0
P2	B0	B0	B0	LG0	LG0	LG0	LB1	LB1
P1	G0	G0	G0			LR3		LB2
P0	R0	R0	R0	LR0	LR0	LR0		LB3

3.7.27 Signal Configuration – TFT Displays

	TFT								
Pin name	9-bit	9-bit x 2	12-bit	12-bit x 2	15-bit	15-bit x 2	18-bit	18-bit x 2	24-bit
P35		B12		B13		B14		B15	
P34	B2	B02	B3	B03	B4	B04		B14	
P33		B11		B12		B13		B13	
P32	B1	B01	B2	B02	B3	B03		B12	
P31		B10		B11		B12		B11	
P30	B0	B00	B1	B01	B2	B02		B10	
P29				B10		B11		G15	
P28			B0	B00	B1	B01		G14	
P27						B10		G13	
P26					B0	B00		G12	
P25								G11	
P24								G10	
P23		G12		G13		G14	R5	R05	R7
P22	G2	G02	G3	G03	G4	G04	R4	R04	R6
P21		G11		G12		G13	R3	R03	R5
P20	G1	G01	G2	G02	G3	G03	R2	R02	R4
P19		G10		G11		G12	R1	R01	R3
P18	G0	G00	G1	G01	G2	G02	R0	R00	R2
P17				G10		G11		R11	R1
P16			G0	G00	G1	G01		R10	R0
P15						G10	G5	G05	G7
P14					G0	G00	G4	G04	G6
P13							G3	G03	G5
P12							G2	G02	G4
P11		R12		R13		R14	G1	G01	G3
P10	R2	R02	R3	R03	R4	R04	G0	G00	G2
P9		R11		R12		R13		R13	G1
P8	R1	R01	R2	R02	R3	R03		R12	G0
P7		R10		R11		R12	B5	B05	B7
P6	R0	R00	R1	R01	R2	R02	B4	B04	B6
P5				R10		R11	B3	B03	B5
P4			R0	R00	R1	R01	B2	B02	B4
P3						R10	B1	B01	B3
P2					R0	R00	B0	B00	B2
P1								R15	B1
P0								R14	B0

Note:

The principle of attachment of TFT panels is that the bits for red, green, and blue use the most significant bits and skip the least significant bits if the display interface width of the TFT panel is insufficient.

3.7.28 Zoom Video Port Connector (CN14)

Signal	PIN		Signal
ZV1	2	1	ZV0
ZV3	4	3	ZV2
ZV5	6	5	ZV4
ZV7	8	7	ZV6
ZV9	10	9	ZV8
ZV11	12	11	ZV10
ZV13	14	13	ZV12
ZV15	16	15	ZV14
ZV-VS	18	17	ZV-HREF
GND	20	19	ZV-LCLK

3.7.29 Signal Description – Zoom Video Port Connector (CN14)

ZV [15:0]	ZV-port data bus. Video input
ZV-LCLK	ZV-port clock
ZV-HREF	ZV-Port Horizontal Sync.
ZV-VS	ZV-Port Vertical Sync.

3.7.30 Floppy Disk Connector (FLP1)

Signal	PIN		Signal
GND	1	2	DRVDEN0#
GND	3	4	NC
GND	5	6	NC
GND	7	8	INDEX#
GND	9	10	MOA#
GND	11	12	DSB#
GND	13	14	DSA#
GND	15	16	MOB#
GND	17	18	DIR#
GND	19	20	STEP#
GND	21	22	WD#
GND	23	24	WE#
GND	25	26	TRAK0#
GND	27	28	WPT#
GND	29	30	RDATA#
GND	31	32	SIDE1#
GND	33	34	DSKCHG#

3.7.31 Signal Description – Floppy Disk Connector (FLP1)

RDATA#	The read data input signal from the FDD.
WD#	Write data. This logic low open drain writes pre-compensation serial data to the selected FDD. An open drain output.
WE#	Write enable. An open drain output.
MOA#	Motor A On. When set to 0, this pin enables disk drive 0. This is an open drain output.
MOB#	Motor B On. When set to 0, this pin enables disk drive 1. This is an open drain output.
DSA#	Drive Select A. When set to 0, this pin enables disk drive A. This is an open drain output.
DSB#	Drive Select B. When set to 0, this pin enables disk drive B. This is an open drain output.
SIDE1#	This output signal selects side of the disk in the selected drive.
DIR#	Direction of the head step motor. An open drain output Logic 1 = outward motion Logic 0 = inward motion
STEP#	Step output pulses. This active low open drain output produces a pulse to move the head to another track.
DRVDEN0#	This output indicates whether a low drive density (250/300kbps at low level) or a high drive density (500/1000kbps at high level) has been selected.
TRAK0#	Track 0. This Schmitt-triggered input from the disk drive is active low when the head is positioned over the outermost track.
INDEX#	This Schmitt-triggered input from the disk drive is active low when the head is positioned over the beginning of a track marked by an index hole.
WP#	Write protected. This active low Schmitt input from the disk drive indicates that the diskette is write-protected.
DSKCHG#	Diskette change. This signal is active low at power on and whenever the diskette is removed.

3.7.32 IrDA Connector (IR1)

Signal	PIN		Signal
ITX	5	6	NC
IRX	3	4	GND
VCC	1	2	NC

3.7.33 Signal Description – IR Connector (IR1)

IRRX	Infrared Receiver input
IRTX	Infrared Transmitter output

3.7.34 Auxiliary Power Connector (J4)

Signal	PIN
VCCSB	3
VCC	2
PSON#	1

Note:
The default sets J4 to 2-3 closed for AT power supply using.

3.7.35 LCD Inverter Connector (J8)

Signal	PIN
VCC	5
VR	4
ENBKL	3
GND	2
+12V	1

Note: For inverters with adjustable Backlight function, it is possible to control the LCD brightness through the VR signal (pin 4) controlled by **VR1**. Please see the VR1 section for detailed circuitry information.

3.7.36 Signal Description – LCD Inverter Connector (J8)

VR	Vadj = 5V ~ 0V.
ENBKL	LCD backlight ON/OFF control signal.

3.7.37 10/100 BASE-Tx Ethernet Connector (LAN1, LAN2 / EBC5612 only)

Signal	PIN
TXD+	1
TXD-	2
RXD+	3
NC	4
NC	5
RXD-	6
NC	7
NC	8

3.7.38 Signal Description – 10/100Base-Tx Ethernet Connector (LAN1, LAN2 / EBC5612 only)

TXD+ / TXD-	Ethernet 10/100Base-Tx differential transmitter outputs.
RXD+ / RXD-	Ethernet 10/100Base-Tx differential receiver inputs.

3.7.39 Parallel Port Connector (PNT1)

Signal	PIN		Signal
STB#	1	2	AFD#
PD0	3	4	ERR#
PD1	5	6	INIT#
PD2	7	8	SLIN#
PD3	9	10	GND
PD4	11	12	GND
PD5	13	14	GND
PD6	15	16	GND
PD7	17	18	GND
ACK#	19	20	GND
BUSY	21	22	GND
PE	23	24	GND
SLCT	25	26	GND

3.7.40 DB25 Parallel Port Connector

Signal	PIN		Signal
STB#	1		
		14	AFD#
PD0	2		
		15	ERR#
PD1	3		
		16	INIT#
PD2	4		
		17	SLIN#
PD3	5		
		18	GND
PD4	6		
		19	GND
PD5	7		
		20	GND
PD6	8		
		21	GND
PD7	9		
		22	GND
ACK#	10		
		23	GND
BUSY	11		
		24	GND
PE#	12		
		25	GND
SLCT	13		

3.7.41 Signal Description – Parallel Port (PNT1)

The following signal description covers the signal definitions, when the parallel port is operated in standard centronic mode. The parallel port controller also supports the fast EPP and ECP modes.

PD [7:0]	Parallel data bus from PC board to printer. The data lines are able to operate in PS/2 compatible bi-directional mode.
SLIN#	Output line for detection of printer selection. This pin is pulled high internally.
SLCT	An active high input on this pin indicates that the printer is selected. This pin is pulled high internally.
STB#	An active low output is used to latch the parallel data into the printer. This pin is pulled high internally.
BUSY	An active high input indicates that the printer is not ready to receive data. This pin is pulled high internally.
ACK#	An active low input on this pin indicates that the printer has received data and is ready to accept more data. This pin is pulled high internally.
INIT#	Output line for the printer initialization. This pin is pulled high internally.
AFD#	An active low output from this pin causes the printer to auto feed a line after a line is printed. This pin is pulled high internally.
ERR#	An active low input on this pin indicates that the printer has encountered an error condition. This pin is pulled high internally.
PE#	An active high input on this pin indicates that the printer has detected the end of the paper. This pin is pulled high internally.

3.7.42 IEEE1394 Port 1 Connector (PORT1)

Signal	PIN		Signal
XTPA0P	6	5	XTPA0M
XTPB0P	4	3	XTPB0M
GND	2	1	+12V

3.7.43 Signal Description – IEEE1394 Port 1 Connector (PORT1)

XTPA0P	Port 1 Twisted Pair A Positive.
XTPA0M	Port 1 Twisted Pair A Negative.
XTPB0P	Port 1 Twisted Pair B Positive.
XTPB0M	Port 1 Twisted Pair B Negative.

3.7.44 IEEE1394 Port 2/3 Connector (PORT2)

Signal	PIN		Signal
+12V	1	2	XTPA2P
GND	3	4	XTPA2M
XTPB1M	5	6	XTPB2P
XTPB1P	7	8	XTPB2M
XTPA1M	9	10	GND
XTPA1P	11	12	+12V

3.7.45 Signal Description – IEEE1394 Port 2/3 Connector (PORT2)

XTPA1P	Port 2 Twisted Pair A Positive.
XTPA1M	Port 2 Twisted Pair A Negative.
XTPB1P	Port 2 Twisted Pair B Positive.
XTPB1M	Port 2 Twisted Pair B Negative.
XTPA2P	Port 3 Twisted Pair A Positive.
XTPA2M	Port 3 Twisted Pair A Negative.
XTPB2P	Port 3 Twisted Pair B Positive.
XTPB2M	Port 3 Twisted Pair B Negative.

3.7.46 Power Connector (PWR1)

Signal	PIN
NC	1
VCC	2
+12V	3
-12V	4
GND	5
GND	6
GND	7
GND	8
-5V	9
VCC	10
VCC	11
VCC	12

3.7.47 USB Connector (USB1)

Signal	PIN CH2	PIN CH1	Signal
VCC1	1	2	GND
D1-	3	4	GND
D1+	5	6	D2+
GND	7	8	D2-
GND	9	10	VCC2

3.7.48 Signal Description – USB Connector (USB1)

D1+ / D1-	Differential bi-directional data signal for USB channel 0. Clock is transmitted along with the data using NRZI encoding. The signalling bit rate is up to 12 Mbs.
D2+ / D2-	Differential bi-directional data signal for USB channel 1. Clock is transmitted along with the data using NRZI encoding. The signalling bit rate is up to 12 Mbs.
VCC	5 V DC supply for external devices. Maximum load according to USB standard.

3.7.49 CRT Connector (VGA1)

Signal	PIN	PIN	Signal
RED	1	9	VCC
GREEN	2	10	GND
BLUE	3	11	NC
NC	4	12	DAT
GND	5	13	HSYNC
GND	6	14	VSYNC
GND	7	15	DCLK
GND	8	16	NC

3.7.50 Signal Description – CRT Connector (VGA1)

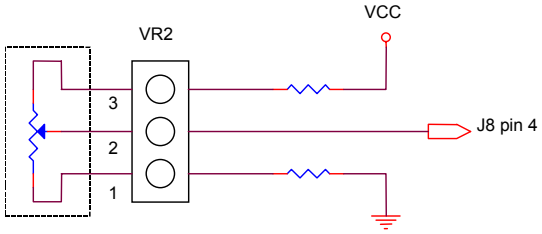
HSYNC	CRT horizontal synchronisation output.
VSYNC	CRT vertical synchronisation output.
DDCCLK	Display Data Channel Clock. Used as clock signal to/from monitors with DDC interface.
DDCDAT	Display Data Channel Data. Used as data signal to/from monitors with DDC interface.
RED	Analog output carrying the red colour signal to the CRT. For 75 Ω cable impedance.
GREEN	Analog output carrying the green colour signal to the CRT. For 75 Ω cable impedance.
BLUE	Analog output carrying the blue colour signal to the CRT. For 75 Ω cable impedance.

3.7.51 STN LCD Contrast Adjustment Connector (VR1)

Signal	PIN
VCC3	3
Vcon	2
GND	1

3.7.52 LCD Backlight Brightness Adjustment Connector (VR2)

Signal	PIN
VCC	3
VBR	2
GND	1



Variation Resistor (Recommended: 4.7KΩ, >1/16W)

4. AWARD BIOS Setup

4.1 Starting Setup

The AwardBIOS™ is immediately activated when you first power on the computer. The BIOS reads the system information contained in the CMOS and begins the process of checking out the system and configuring it. When it finishes, the BIOS will seek an operating system on one of the disks and then launch and turn control over to the operating system.

While the BIOS is in control, the Setup program can be activated in one of two ways:

By pressing <Del> immediately after switching the system on, or

By pressing the <Del> key when the following message appears briefly at the bottom of the screen during the POST (Power On Self Test).

```
Press DEL to enter SETUP
```

If the message disappears before you respond and you still wish to enter Setup, restart the system to try again by turning it OFF then ON or pressing the "RESET" button on the system case. You may also restart by simultaneously pressing <Ctrl>, <Alt>, and <Delete> keys. If you do not press the keys at the correct time and the system does not boot, an error message will be displayed and you will again be asked to.

```
Press F1 To Continue, DEL to enter SETUP
```

4.2 Using Setup

In general, you use the arrow keys to highlight items, press <Enter> to select, use the PageUp and PageDown keys to change entries, press <F1> for help and press <Esc> to quit. The following table provides more detail about how to navigate in the Setup program using the keyboard.

Up arrow	Move to previous item
Down arrow	Move to next item
Left arrow	Move to the item in the left hand
Right arrow	Move to the item in the right hand
Esc key	Main Menu -- Quit and not save changes into CMOS Status Page Setup Menu and Option Page Setup Menu -- Exit current page and return to Main Menu
PgUp key	Increase the numeric value or make changes
PgDn key	Decrease the numeric value or make changes
+ key	Increase the numeric value or make changes
- key	Decrease the numeric value or make changes
F1 key	General help, only for Status Page Setup Menu and Option Page Setup Menu
(Shift) F2 key	Change color from total 16 colors. F2 to select color forward, (Shift) F2 to select color backward
F3 key	Calendar, only for Status Page Setup Menu
F4 key	Reserved
F5 key	Restore the previous CMOS value from CMOS, only for Option Page Setup Menu
F6 key	Load the default CMOS value from BIOS default table, only for Option Page Setup Menu
F7 key	Load the default
F8 key	Reserved
F9 key	Reserved
F10 key	Save all the CMOS changes, only for Main Menu

Table 1 : Legend Keys

4.2.1 Navigating Through The Menu Bar

Use the left and right arrow keys to choose the menu you want to be in.

4.2.2 To Display a Sub Menu

Use the arrow keys to move the cursor to the sub menu you want. Then press <Enter>. A "➢" pointer marks all sub menus.

4.3 Getting Help

Press F1 to pop up a small help window that describes the appropriate keys to use and the possible selections for the highlighted item. To exit the Help Window press <Esc> or the F1 key again.

4.4 In Case of Problems

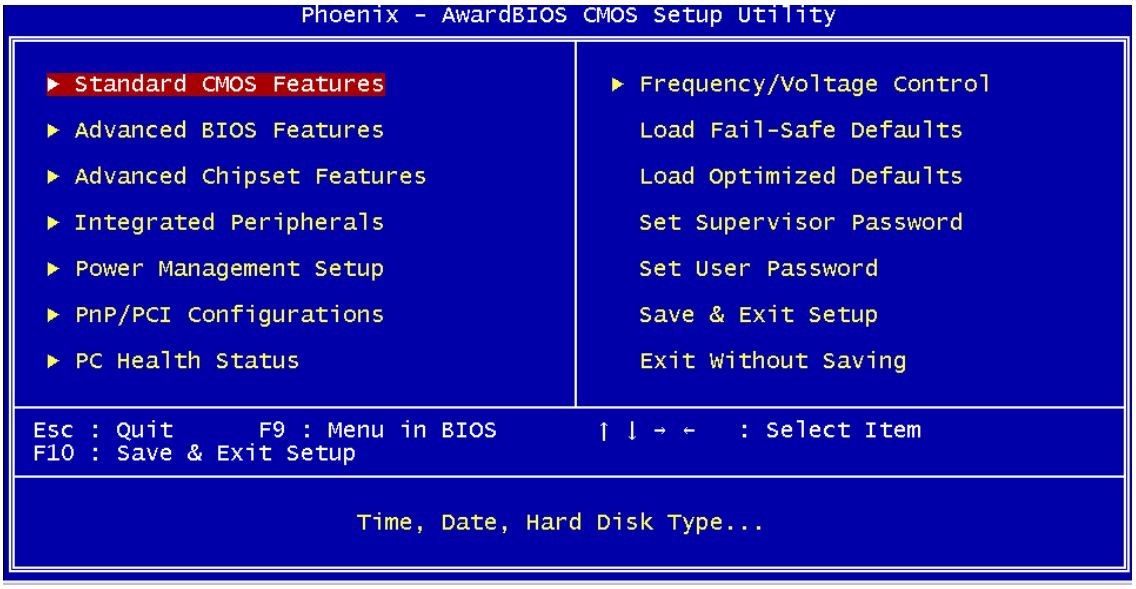
If, after making and saving system changes with Setup, you discover that your computer no longer is able to boot, the AwardBIOS™ supports an override to the CMOS settings which resets your system to its defaults.

The best advice is to only alter settings which you thoroughly understand. To this end, we strongly recommend that you avoid making any changes to the chipset defaults. These defaults have been carefully chosen by both Award and your systems manufacturer to provide the absolute maximum performance and reliability. Even a seemingly small change to the chipset setup has the potential for causing you to use the override.

4.5 Main Menu

Once you enter the AwardBIOS™ CMOS Setup Utility, the Main Menu will appear on the screen. The Main Menu allows you to select from several setup functions and two exit choices. Use the arrow keys to select among the items and press <Enter> to accept and enter the sub-menu.

Note that a brief description of each highlighted selection appears at the bottom of the screen.



4.5.1 Setup Items

The main menu includes the following main setup categories. Recall that some systems may not include all entries.

4.5.1.1 Standard CMOS Features

Use this menu for basic system configuration.

4.5.1.2 Advanced BIOS Features

Use this menu to set the Advanced Features available on your system.

4.5.1.3 Advanced Chipset Features

Use this menu to change the values in the chipset registers and optimize your system's performance.

4.5.1.4 Integrated Peripherals

Use this menu to specify your settings for integrated peripherals.

4.5.1.5 Power Management Setup

Use this menu to specify your settings for power management.

4.5.1.6 PNP / PCI Configuration

This entry appears if your system supports PnP / PCI.

4.5.1.7 PC Health Status

This entry appears your system Hardware Monitor Status

4.5.1.8 Frequency / Voltage Control

Use this menu to specify your settings for frequency/voltage control.

4.5.1.9 Load Fail-Safe Defaults

Use this menu to load the BIOS default values for the minimal/stable performance for your system to operate.

4.5.1.10 Load Optimized Defaults

Use this menu to load the BIOS default values that are factory settings for optimal performance system operations. While Award has designed the custom BIOS to maximize performance, the factory has the right to change these defaults to meet their needs.

4.5.1.11 Supervisor / User Password

Use this menu to set User and Supervisor Passwords.

4.5.1.12 Save & Exit Setup

Save CMOS value changes to CMOS and exit setup.

4.5.1.13 Exit Without Save

Abandon all CMOS value changes and exit setup.

4.5.2 Standard CMOS Setup

The items in Standard CMOS Setup Menu are divided into 10 categories. Each category includes no, one or more than one setup items. Use the arrow keys to highlight the item and then use the <PgUp> or <PgDn> keys to select the value you want in each item.

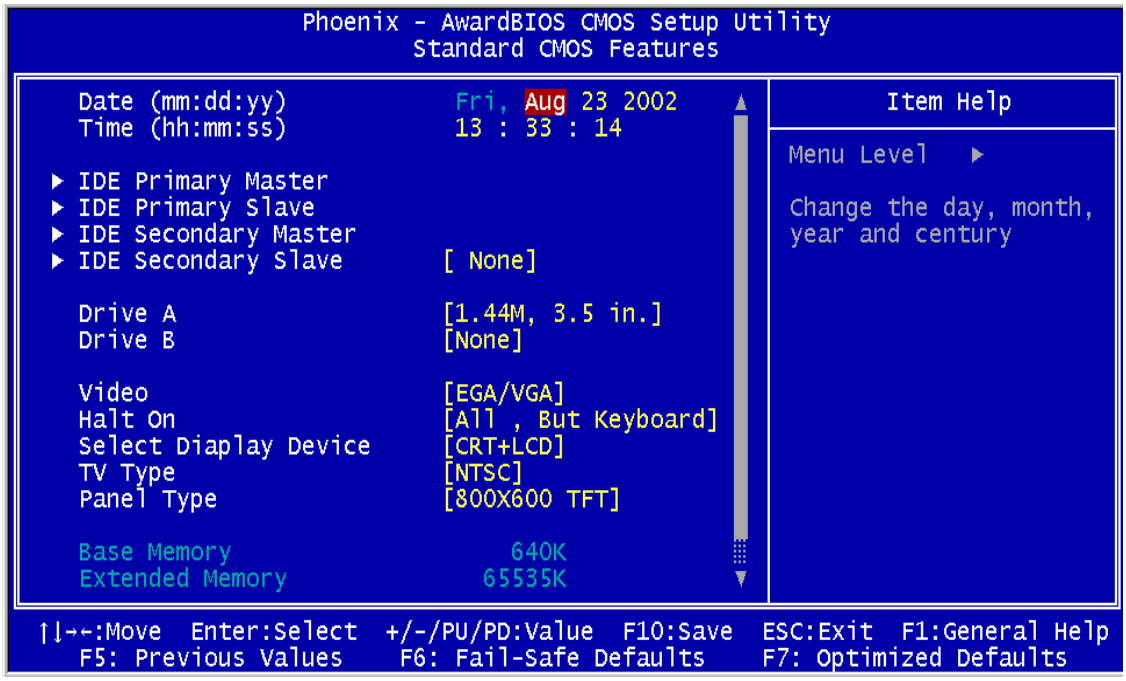


Figure 1 : The Main Menu

4.5.2.1 Main Manu Selection

This table shows the selections that you can make on the Main Menu.

Item	Options	Description
Date	Month DD YYYY	Set the system date. Note that the 'Day' automatically changes when you set the date
Time	HH : MM : SS	Set the system time
IDE Primary Master	Options are in its sub menu (described in Table 3)	Press <Enter> to enter the sub menu of detailed options
IDE Primary Slave	Options are in its sub menu (described in Table 3)	Press <Enter> to enter the sub menu of detailed options
IDE Secondary Master	Options are in its sub menu (described in Table 3)	Press <Enter> to enter the sub menu of detailed options
IDE Secondary Master	Options are in its sub menu (described in Table 3)	Press <Enter> to enter the sub menu of detailed options
Drive A Drive B	None 360K, 5.25 in 1.2M, 5.25 in 720K, 3.5 in 1.44M, 3.5 in 2.88M, 3.5 in	Select the type of floppy disk drive installed in your system
Video	EGA/VGA CGA 40 CGA 80 MONO	Select the default video device
Halt On	All Errors No Errors All, but Keyboard All, but Diskette All, but Disk/Key	Select the situation in which you want the BIOS to stop the POST process and notify you

Select Display Device	Auto CRT LCD CRT+LCD TV CRT+TV	Select the Display Device
TV Type	NTSC PAL	Select the TV Format
Panel Type	640x480 TFT 800x600 TFT 1024x768 TFT 2P/C32M 1280x1024 TFT 640x480 DSTN 800x600 DSTN 1024x768 DSTN 1024x768 TFT 1P/C65M 640x480 TFT 800x600 TFT 1024x768 TFT 1280x1024 TFT 1400x1050 TFT 2P/C54M 800x600 DSTN 1024x768 DSTN 1280x1024 DSTN	Panel Type
Base Memory	N/A	Displays the amount of conventional memory detected during boot up
Extended Memory	N/A	Displays the amount of extended memory detected during boot up
Total Memory	N/A	Displays the total memory available in the system

Table 2 : Main Menu Selections

4.5.2.2 IDE Adapters

The IDE adapters control the hard disk drive. Use a separate sub menu to configure each hard disk drive.

Figure 2 shows the IDE primary master sub menu.

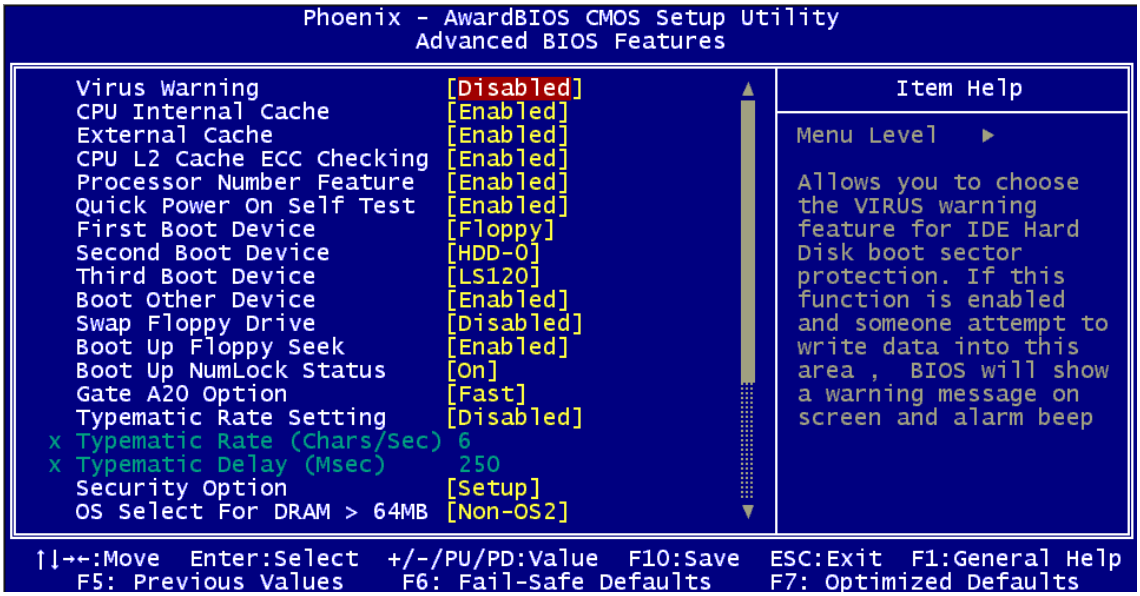
Use the legend keys to navigate through this menu and exit to the main menu. Use Table 3 to configure the hard disk.

Item	Options	Description
IDE HDD Auto-detection	Press Enter	Press Enter to auto-detect the HDD on this channel. If detection is successful, it fills the remaining fields on this menu.
IDE Primary Master	None Auto Manual	Selecting 'manual' lets you set the remaining fields on this screen. Selects the type of fixed disk. "User Type" will let you select the number of cylinders, heads, etc. Note: PRECOMP=65535 means NONE !
Capacity	Auto Display your disk drive size	Disk drive capacity (Approximated). Note that this size is usually slightly greater than the size of a formatted disk given by a disk checking program.
Access Mode	Normal LBA Large Auto	Choose the access mode for this hard disk
The following options are selectable only if the 'IDE Primary Master' item is set to 'Manual'		
Cylinder	Min = 0 Max = 65535	Set the number of cylinders for this hard disk.
Head	Min = 0 Max = 255	Set the number of read/write heads
Precomp	Min = 0 Max = 65535	**** **Warning**: Setting a value of 65535 means no hard disk
Landing zone	Min = 0 Max = 65535	****
Sector	Min = 0 Max = 255	Number of sectors per track

Table 3 : Hard disk selections

4.5.3 Advanced BIOS Features

This section allows you to configure your system for basic operation. You have the opportunity to select the system's default speed, boot-up sequence, keyboard operation, shadowing and security.



4.5.3.1 Virus Warning

This item allows you to choose the VIRUS Warning feature for IDE Hard Disk boot sector protection. If this function is enabled and someone attempt to write data into this area, BIOS will show a warning message on screen and alarm beep.

Enabled	Activates automatically when the system boots up causing a warning message to appear when anything attempts to access the boot sector or hard disk partition table.
Disabled	No warning message will appear when anything attempts to access the boot sector or hard disk partition table.

4.5.3.2 CPU Internal Cache

This item allows you to speed up memory access. However, it depends on CPU design.

Enabled	Enable cache
Disabled	Disable cache

4.5.3.3 External Cache

This item allows you to speed up memory access. However, it depends on chipset design.

Enabled	Enable cache
Disabled	Disable cache

4.5.3.4 CPU L2 Cache ECC Checking

This item allows you to enable/disable CPU L2 Cache ECC checking.

Enabled	Enable L2 Cache ECC Checking
Disabled	Disable L2 Cache ECC Checking

4.5.3.5 Quick Power On Self Test

This category speeds up Power On Self Test (POST) after you power up the computer. If it is set to Enable, BIOS will shorten or skip some check items during POST.

Enabled	Enable quick POST
Disabled	Normal POST

4.5.3.6 First/Second/Third/Other Boot Device

The BIOS attempts to load the operating system from the devices in the sequence selected in these items.

Floppy	Floppy Device
LS120	LS120 Device
HDD-0	First Hard Disk Device
SCSI	SCSI Device
CDROM	CDROM Device
HDD-1	Secondary Hard Disk Device
HDD-2	Third Hard Disk Device
HDD-3	Fourth Hard Disk Device
ZIP100	ZIP-100 Device
USB-FDD	USB Floppy Device
USB-ZIP	USB ZIP Device
USB-CDROM	USB CDROM Device
USB-HDD	USB Hard Disk Device
LAN	Network Device
Disabled	Disabled any boot device

4.5.3.7 Boot Up Floppy Seek

Seeks disk drives during boot up. Disabling speeds boot up.

Enabled	Enable Floppy Seek
Disabled	Disable Floppy Seek

4.5.3.8 Boot Up NumLock Status

Select power on state for NumLock.

Enabled	Enable NumLock
Disabled	Disable NumLock

4.5.3.9 Gate A20 Option

Select if chipset or keyboard controller should control GateA20.

Normal	A pin in the keyboard controller controls GateA20
Fast	Lets chipset control GateA20

4.5.3.10 Typematic Rate Setting

Key strokes repeat at a rate determined by the keyboard controller. When enabled, the typematic rate and typematic delay can be selected.

The choice: Enabled/Disabled.

4.5.3.11 Typematic Rate (Chars/Sec)

Sets the number of times a second to repeat a key stroke when you hold the key down.

The choice: 6, 8, 10, 12, 15, 20, 24, or 30.

4.5.3.12 Typematic Delay (Msec)

Sets the delay time after the key is held down before it begins to repeat the keystroke.

The choice: 250, 500, 750, or 1000.

4.5.3.13 Security Option

Select whether the password is required every time the system boots or only when you enter setup.

System	The system will not boot and access to Setup will be denied if the correct password is not entered at the prompt.
Setup	The system will boot, but access to Setup will be denied if the correct password is not entered at the prompt.

Note: To disable security, select PASSWORD SETTING at Main Menu and then you will be asked to enter password. Do not type anything and just press <Enter>, it will disable security. Once the security is disabled, the system will boot and you can enter Setup freely.

4.5.3.14 OS Select for DRAM > 64MB

Select the operating system that is running with greater than 64MB of RAM on the system.

The choice: Non-OS2, OS2.

4.5.3.15 Video BIOS Shadow

Determines whether video BIOS will be copied to RAM. However, it is optional depending on chipset design. Video Shadow will increase the video speed.

Enabled	Video shadow is enabled
Disabled	Video shadow is disabled

4.5.3.16 C8000 – CBFFF Shadow/DC000 – DFFFF Shadow

These categories determine whether option ROMs will be copied to RAM. An example of such option ROM would be support of on-board SCSI.

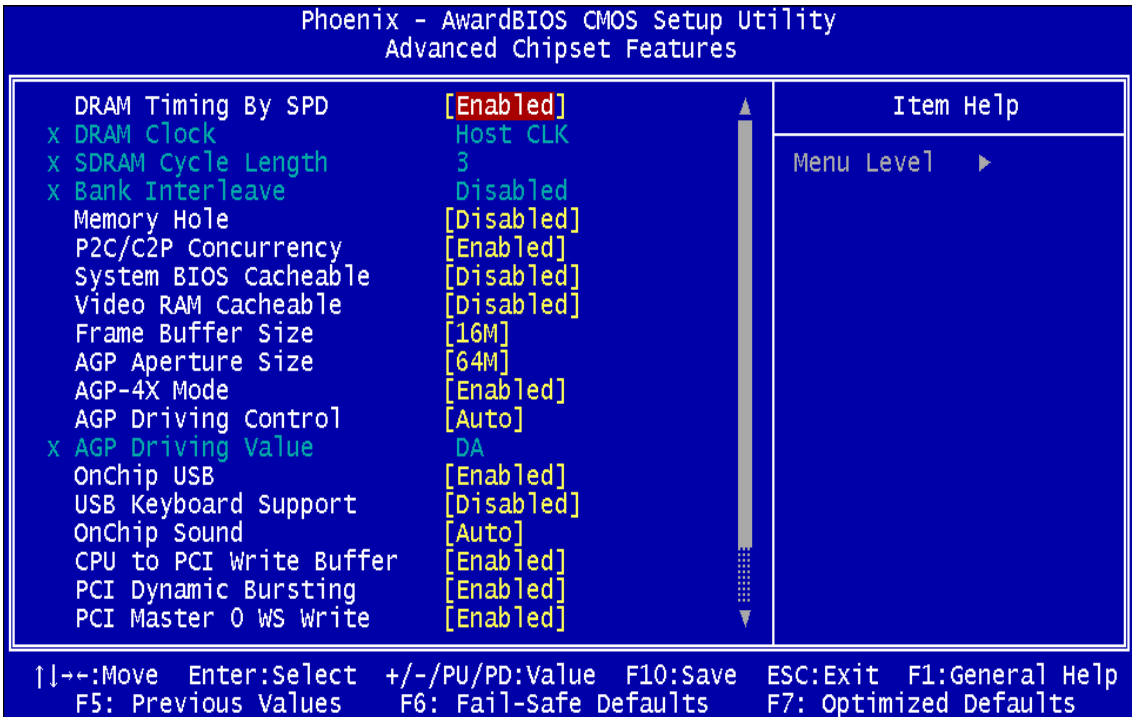
Enabled	Optional shadow is enabled
Disabled	Optional shadow is disabled

4.5.3.17 Small Logo (EPA) Show

This item allows you enabled/disabled the small EPA logo show on screen at the POST step,

Enabled	EPA Logo show is enabled
Disabled	EPA Logo show is disabled

4.5.4 Advanced Chipset Features



This section allows you to configure the system based on the specific features of the installed chipset. This chipset manages bus speeds and access to system memory resources, such as DRAM and the external cache. It also coordinates communications between the conventional ISA bus and the PCI bus. It must be stated that these items should never need to be altered. The default settings have been chosen because they provide the best operating conditions for your system. The only time you might consider making any changes would be if you discovered that data was being lost while using your system.

The first chipset settings deal with CPU access to dynamic random access memory (DRAM). The default timings have been carefully chosen and should only be altered if data is being lost. Such a scenario might well occur if your system had mixed speed DRAM chips installed so that greater delays may be required to preserve the integrity of the data held in the slower memory chips.

4.5.4.1 DRAM Timing by SPD

This item allows you to select the SDRAM timing value by SPD data.

The Choice: Enabled, Disabled.

4.5.4.2 DRAM Clock

This item allows you to set DRAM clock speed.

The Choice: Host CLK, HCLK-33M, HCLK+33M.

4.5.4.3 SDRAM Cycle Length

When synchronous DRAM is installed, the number of clock cycles of CAS latency depends on the DRAM timing. Do not reset this field from the default value specified by the system designer.

The Choice: 2, 3.

4.5.4.4 Bank Interleave

Set SDRAM bank interleaves.

The Choice: Disabled, 2 Banks or 4 Banks.

4.5.4.5 Memory Hole

In order to improve performance, certain space in memory is reserved for ISA cards. This memory must be mapped into the memory space below 16MB.

The Choice: 15M-16M, Disabled.

4.5.4.6 P2C/C2P Concurrency

When disabled, CPU bus will be occupied during the entire PCI operation period.

The Choice: Enabled, Disabled.

4.5.4.7 System BIOS Cacheable

Selecting *Enabled* allows caching of the system BIOS ROM at F0000h-FFFFFh, resulting in better system performance. However, if any program writes to this memory area, a system error may result.

The choice: Enabled, Disabled.

4.5.4.8 Video RAM Cacheable

Select Enabled allows caching of the video RAM, resulting in better system performance. However, if any program writes to this memory area, a system error may result.

The Choice: Enabled, Disabled.

4.5.4.9 Frame Buffer Size

Select the size of onboard video controller's frame buffer. The buffer size is share from system memory unit.

The Choice: 2M, 4M, 8M, 16M, 32M.

4.5.4.10 AGP Aperture Size

Select the size of Accelerated Graphics Port (AGP) aperture. The aperture is a portion of the PCI memory address range dedicated for graphics memory address space. Host cycles that hit the aperture range are forwarded to the AGP without any translation.

The Choice: 4M, 8M, 16M, 32M, 64M, 128M

4.5.4.11 AGP-4X Mode

This item allows you to enable / disable the AGP-4X Mode.

The Choice: Enabled, Disabled.

4.5.4.12 AGP Driving Control

This item allows you to select the AGP Driving Control to auto / disable Mode.

The Choice: Auto, Disabled.

4.5.4.13 AGP Driving Value

This item allows you to set the AGP Driving value.

The Choice: 00 ~ FF (Hex)

4.5.4.14 OnChip USB

This should be enabled if your system has a USB installed on the system board and you wish to use it. Even when so equipped, if you add a higher performance controller, you will need to disable this feature.

The choice: Enabled, Disabled.

4.5.4.15 USB Keyboard Support

Select *Enabled* if your system contains a Universal Serial Bus (USB) controller and you have a USB keyboard that want to using in DOS mode.

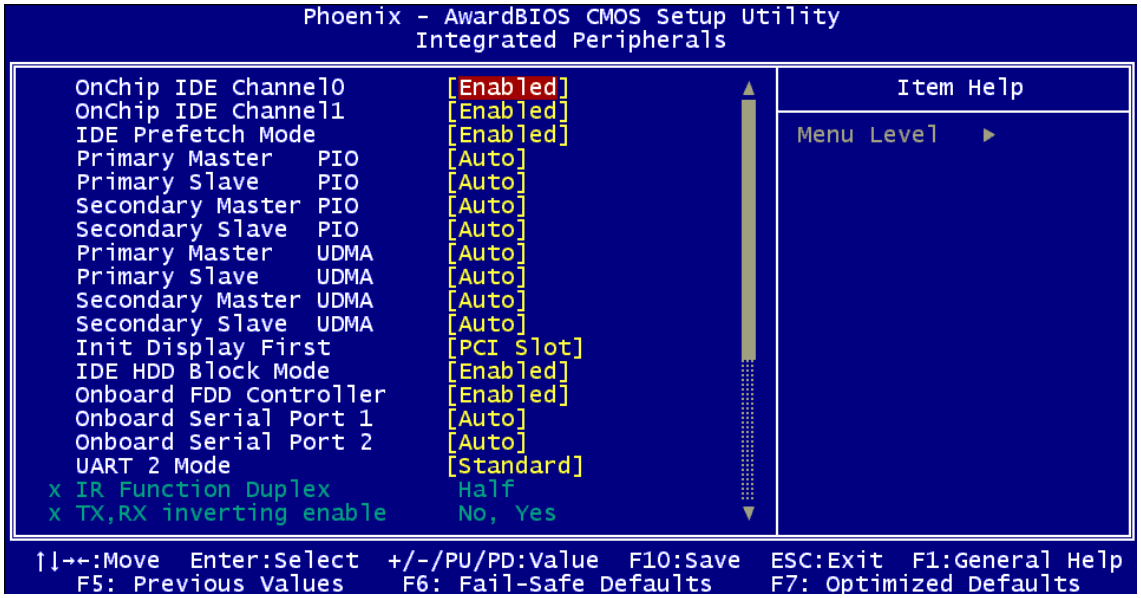
The choice: Enabled, Disabled.

4.5.4.16 OnChip Sound

Select *Enabled* to use the audio capabilities of your system. Most of the following fields do not appear when this field is *Disabled.*

The Choice: Auto, Disabled.

4.5.5 Integrated Peripherals



4.5.5.1 OnChip IDE Channel 0

The chipset contains a PCI IDE interface with support for two IDE channels. Select Enabled to activate the primary IDE interface. Select Disabled to deactivate this interface.

The choice: Enabled, Disabled.

4.5.5.2 OnChip IDE Channel 1

The chipset contains a PCI IDE interface with support for two IDE channels. Select Enabled to activate the secondary IDE interface. Select Disabled to deactivate this interface.

The choice: Enabled, Disabled.

4.5.5.3 IDE Prefetch Mode

The onboard IDE drive interfaces supports IDE prefetching, for faster drive accesses. If you install a primary and/or secondary add-in IDE interface, set this field to *Disabled* if the interface does not support prefetching.

The choice: Enabled, Disabled.

4.5.5.4 Primary/Secondary Master/Slave PIO

The four IDE PIO (Programmed Input/Output) fields let you set a PIO mode (0-4) for each of the four IDE devices that the onboard IDE interface supports. Modes 0 through 4 provide successively increased performance. In Auto mode, the system automatically determines the best mode for each device.

The choice: Auto, Mode 0, Mode 1, Mode 2, Mode 3, or Mode 4.

4.5.5.5 Primary/Secondary Master/Slave UDMA

Ultra DMA/33 implementation is possible only if your IDE hard drive supports it and the operating environment includes a DMA driver (Windows 95 OSR2 or a third-party IDE bus master driver). If your hard drive and your system software both support Ultra DMA/33, select Auto to enable BIOS support.

The Choice: Auto, Disabled.

4.5.5.6 Init Display First

This item allows you to decide to active whether PCI Slot or AGP first.

The choice: PCI Slot, AGP.

4.5.5.7 IDE HDD Block Mode

Block mode is also called block transfer, multiple commands, or multiple sector read/write. If your IDE hard drive supports block mode (most new drives do), select Enabled for automatic detection of the optimal number of block read/writes per sector the drive can support.

The Choice: Enabled, Disabled.

4.5.5.8 Onboard FDC Controller

Select Enabled if your system has a floppy disk controller (FDC) installed on the system board and you wish to use it. If you install and-in FDC or the system has no floppy drive, select Disabled in this field.

The Choice: Enabled, Disabled.

4.5.5.9 Onboard Serial Port 1/Port2

Select an address and corresponding interrupt for the first and second serial ports.

The choice: 3F8/IRQ4, 2E8/IRQ3, 3E8/IRQ4, 2F8/IRQ3, Disabled, Auto.

4.5.5.10 UART 2 Mode

Select UART 2 mode as standard serial port or IR port.

The choice: Standard, ASKIR, HPSIR.

4.5.5.11 IR Function Duplex

Select the value required by the IR device connected to the IR port. Full-duplex mode permits simultaneous two-direction transmission. Half-duplex mode permits transmission in one direction only at a time.

The Choice: Half, Full.

4.5.5.12 TX, RX Inverting Enable

This item allows you to determine the active of RxD, TxD level.

The Choice: Yes, No No, Yes No, No Yes, Yes

4.5.5.13 Onboard Parallel Port

Select a logical LPT port name and matching address for the physical parallel (printer) port.

The choice: 378H/IRQ7, 278H/IRQ5, 3BCH/IRQ7, Disabled.

4.5.5.14 Onboard Parallel Mode

Select an operating mode for the onboard parallel port. Select Compatible or Extended unless you are certain both your hardware and software support EPP or ECP mode.

The choice: EPP, ECP, ECP/EPP, Normal,

4.5.5.15 ECP Mode Use DMA

Select a DMA channel for the port.

The choice: 3, 1.

4.5.5.16 Parallel Port EPP Type

Select EPP port type 1.7 or 1.9.

The choice: EPP1.7, EPP1.9.

4.5.5.17 Onboard Serial Port 3/4

Select an address and corresponding interrupt for the third and forth serial ports.

The choice: (Address) 3F8, 2F8, 3E8, 2E8, Disabled.

(IRQ) IRQ5, IRQ10.

4.5.5.18 Onboard Legacy Audio

This item allows you to enable or disable the onboard legacy audio function.

The choice: Enable, Disable.

4.5.5.19 Sound Blaster

This item allows you to enable or disable the onboard audio function is compatible with sound blaster mode.

The choice: Enable, Disable.

4.5.5.20 SB I/O Base Address

This chipset traps I/O accesses for Sound Blaster compatibility at 220H, 240H, 260H, or 280H.

The choice: 220H, 240H, 260H, 280H.

4.5.5.21 SB IRQ Select

Select an interrupt for the audio port.

The choice: IRQ 5, IRQ 7, IRQ 9, IRQ 10.

4.5.5.22 SB DMA Select

This chipset supports I/O trapping for DMA accesses and allows you to select the Audio DMA type.

The choice: DMA 0, DMA 1, DMA 2, DMA 3.

4.5.5.23 MPU-401

This item allows you to enable or disable MPU-401 function.

The choice: Enable, Disable.

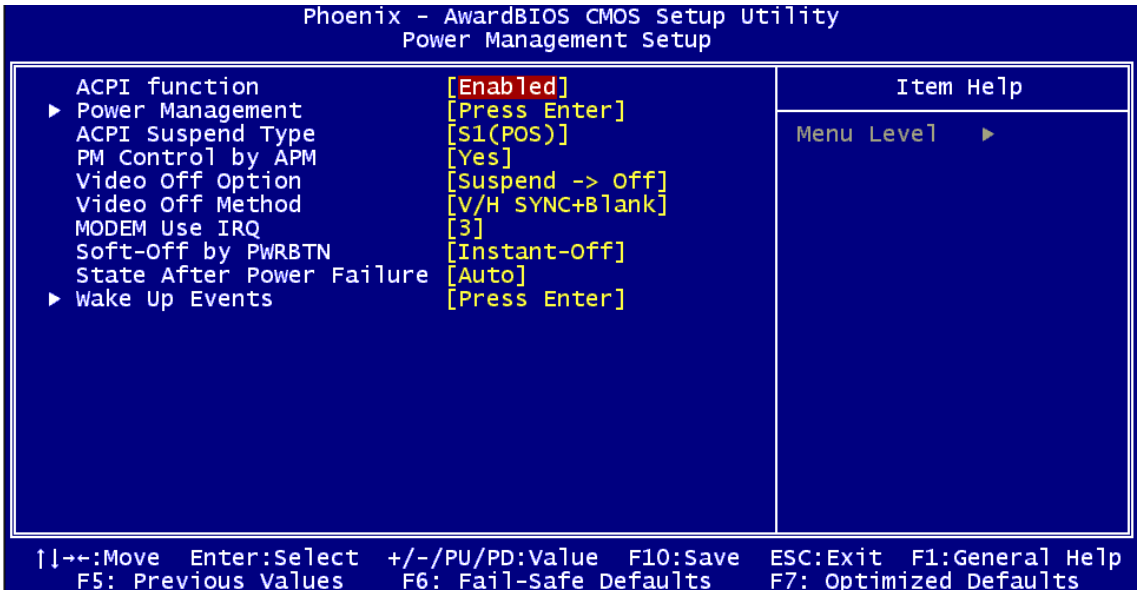
4.5.5.24 MPU-401 I/O Base Address

This chipset traps I/O accesses for ROLAND MPU 401 UART interface at 330H, 300H, or Disable.

The choice: 300-303H, 310-313H, 320-323H, 330-333H.

4.5.6 Power Management Setup

The Power Management Setup allows you to configure you system to most effectively save energy while operating in a manner consistent with your own style of computer use.



4.5.6.1 ACPI Function

This item allows you to enable/disable the ACPI function.

The choice: Enable, Disable.

4.5.6.2 Power Management

This category allows you to select the type (or degree) of power saving and is directly related to the following modes:

1. HDD Power Down
2. Doze Mode
3. Suspend Mode

There are three selections for Power Management, both of them have fixed mode settings.

Min. Power Saving	Minimum power management, HDD Power Down = Disabled, Doze Mode = 1 Hour Suspend Mode = 1 Hour
Max. Power Saving	Maximum power management, HDD Power Down = Disabled, Doze Mode = 1 Min Suspend Mode = 1 Min
User Defined	Allows you to set each mode individually. When not disabled, each of the ranges are from 1 min. to 1 hr. except for HDD Power Down which ranges from 1 min. to 15 min. and disable.

4.5.6.3 PM Control by APM

This item allows you to enable/disable the Advanced Power Management (APM) function.

The choice: Yes, No.

4.5.6.4 Video Off Method

This determines the manner in which the monitor is blanked.

V/H SYNC+Blank	This selection will cause the system to turn off the vertical and horizontal synchronization ports and write blanks to the video buffer.
Blank Screen	This option only writes blanks to the video buffer.
DPMS	Initial display power management signaling.

4.5.6.5 MODEM Use IRQ

This determines the IRQ in which the MODEM can use.

The choice: 3, 4, 5, 7, 9, 10, 11, or NA.

4.5.6.6 Soft-Off by PWRBTN

Pressing the power button for more than 4 seconds forces the system to enter the Soft-Off state when the system has "hung".(Only could working on ATX Power supply)

The choice: Delay 4 Sec, Instant-Off.

4.5.6.7 Wake up Events

PM Wake up events are I/O events whose occurrence can prevent the system from entering a power saving mode or can awaken the system from such a mode. In effect, the system remains alert for anything occurs to a device which is configured as *On*, even when the system is in a power down mode.

4.5.6.7.1 VGA

When *ON,* your can set the LAN awakens the system.

4.5.6.7.2 LPT & COM

When *select* LPT/COM, any activity from one of the listed system peripheral devices or IRQs wakes up the system.

4.5.6.7.3 HDD & FDD

When *On of HDD* & FDD, any activity from one of the listed system peripheral devices wakes up the system.

4.5.6.7.4 PCI Master

When you *are On of PCI Master,* any activity from one of the list system peripheral devices wakes up the system.

4.5.6.8 Power On by PCI Card

This item allows you to determine that does any activity from one of the list system peripheral devices wakes up the system.

The Choice. Enable, Disabled.

4.5.6.8.1 Modem Ring Resume

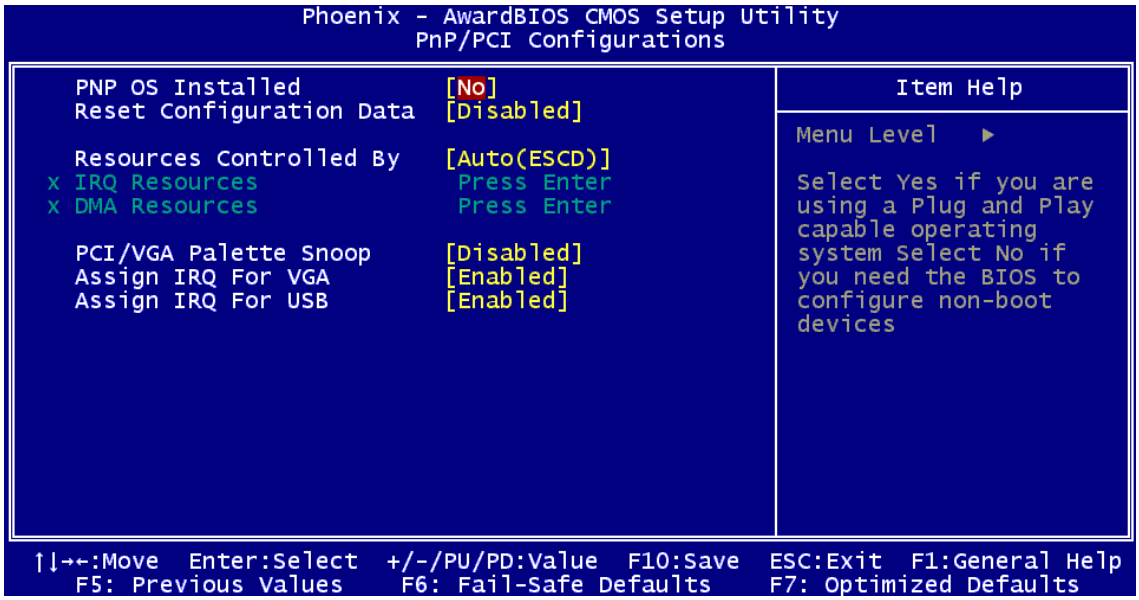
An input signal on the serial Ring Indicator (RI) line (in other words, an incoming call on the modem) awakens the system from a soft off state.

4.5.6.8.2 Disable RTC Alarm Function

When *Enabled,* your can set the date and time at which the RTC (real-time clock) alarm awakens the system from Suspend mode.

4.5.7 PnP/PCI Configuration Setup

This section describes configuring the PCI bus system. PCI, or **P**ersonal **C**omputer **I**nterconnect, is a system allows I/O devices to operate at speeds nearing the speed the CPU itself uses when communicating with its own special components. This section covers some very technical items and it is strongly recommended that only experienced users should make any changes to the default settings.



4.5.7.1 PnP OS Installed

This item allows you to determine install PnP OS or not.

The choice: Yes, No.

4.5.7.2 Reset Configuration Data

Normally, you leave this field Disabled. Select Enabled to reset Extended System Configuration Data (ESCD) when you exit Setup if you have installed a new add-on and the system reconfiguration has caused such a serious conflict that the operating system cannot boot.

The choice: Enabled, Disabled.

4.5.7.3 Resource Controlled by

The Award Plug and Play BIOS has the capacity to automatically configure all of the boot and Plug and Play compatible devices. However, this capability means absolutely nothing unless you are using a Plug and Play operating system such as Windows®95. If you set this field to “manual” choose specific resources by going into each of the sub menu that follows this field (a sub menu is preceded by a “➢”).

The choice: Auto, Manual.

4.5.7.4 IRQ Resources

When resources are controlled manually, assign each system interrupt a type, depending on the type of device using the interrupt.

4.5.7.5 IRQ3/4/5/7/9/10/11/12/14/15 Assigned to

This item allows you to determine the IRQ assigned to the ISA bus and is not available to any PCI slot. Legacy ISA for devices compliant with the original PC AT bus specification, PCI/ISA PnP for devices compliant with the Plug and Play standard whether designed for PCI or ISA bus architecture.

The Choice: *Legacy ISA* and *PCI/ISA PnP*.

4.5.7.6 DMA Resources

When resources are controlled manually, assign each system DMA channel a type, depending on the type of device using the DMA channel.

4.5.7.7 DMA 0/1/3/5/6/7 Assigned to

Legacy ISA for devices compliant with the original PC AT bus specification, PCI/ISA PnP for devices compliant with the Plug and Play standard whether designed for PCI or ISA bus architecture.

Choices are *Legacy ISA* and *PCI/ISA PnP*.

4.5.7.8 PCI / VGA Palette Snoop

Leave this field at *Disabled*.

Choices are Enabled, Disabled.

4.5.7.9 Assign IRQ for VGA

This item allows you to Enable or Disable assign an IRQ for onboard VGA controller.

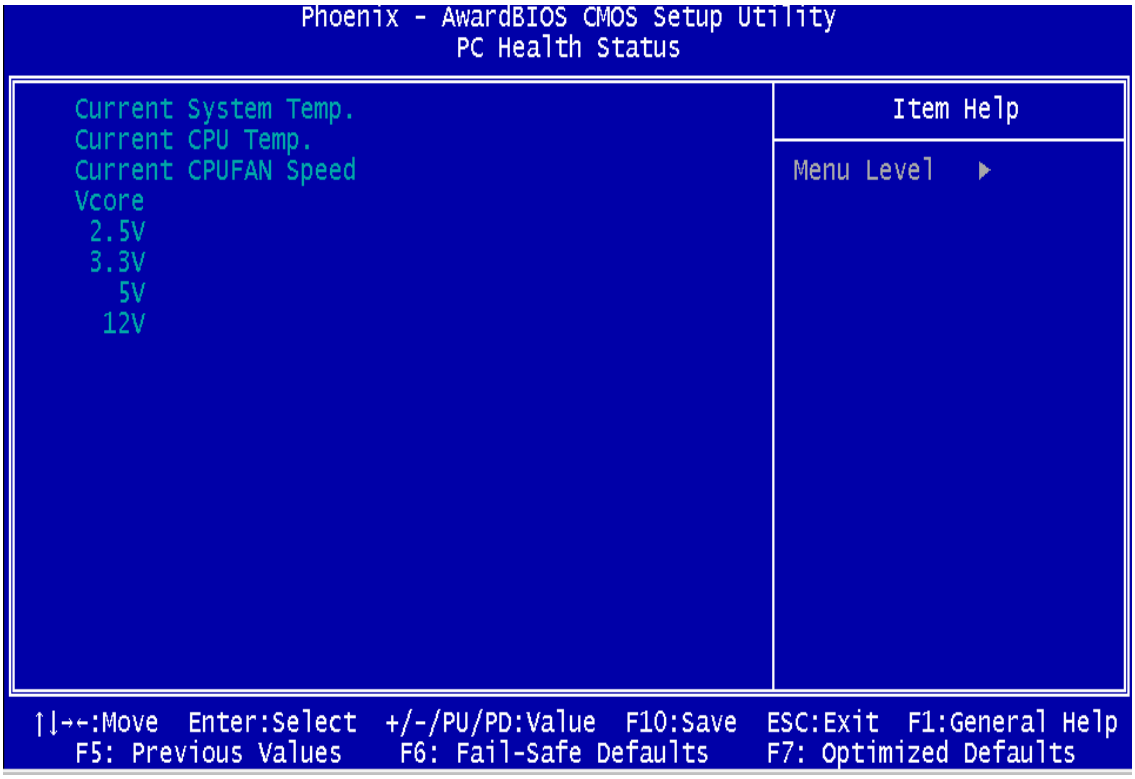
The Choices : Enabled, Disabled.

4.5.7.10 Assign IRQ for USB

This item allows you to Enable or Disable assign an IRQ for onboard USB Controller.

The Choices : Enabled, Disabled.

4.5.8 PC Health Status



4.5.8.1 Current System Temp.

Detect System Temp.automatically

4.5.8.2 Current CPU Temp.

Detect CPU Temp.automatically

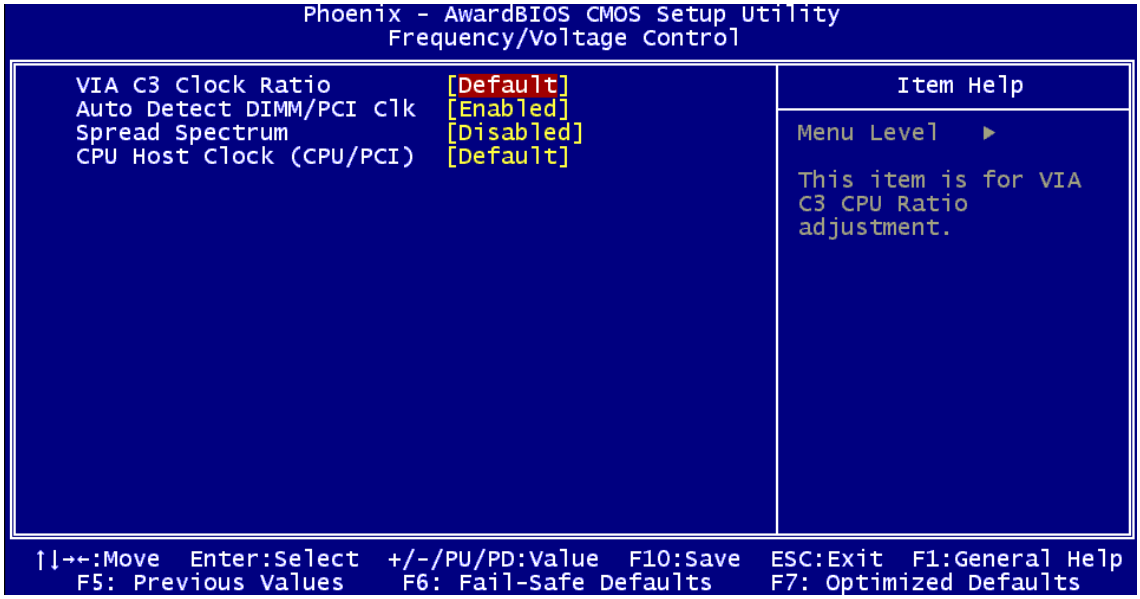
4.5.8.3 Current CPUFAN Speed

Detect CPU FAN speed automatically

4.5.8.4 Current Voltage (V) Vcore/2.5V/3.3V/5V/12V

Detect system's voltage status automatically.

4.5.9 Frequency / Voltage Control



4.5.9.1 VIA C3 Clock Ratio

This item allows you to select the VIA C3 CPU clock ratio.

4.5.9.2 Auto Detect DIMM/ PCI Clk

This item allows you to enable/disable auto detect DIMM/PCI Clock.

The choice: Enable, Disable.

4.5.9.3 Spread Spectrum

This item allows you to enabled Spread Spectrum Modulated.

The choice: Enable, Disable.

4.5.9.4 CPU Host Clock (CPU / PCI)

This item allows you to select the CPU host clock frequency.

4.5.10 Load Fail-Safe Defaults

When you press <Enter> on this item you get a confirmation dialog box with a message similar to:

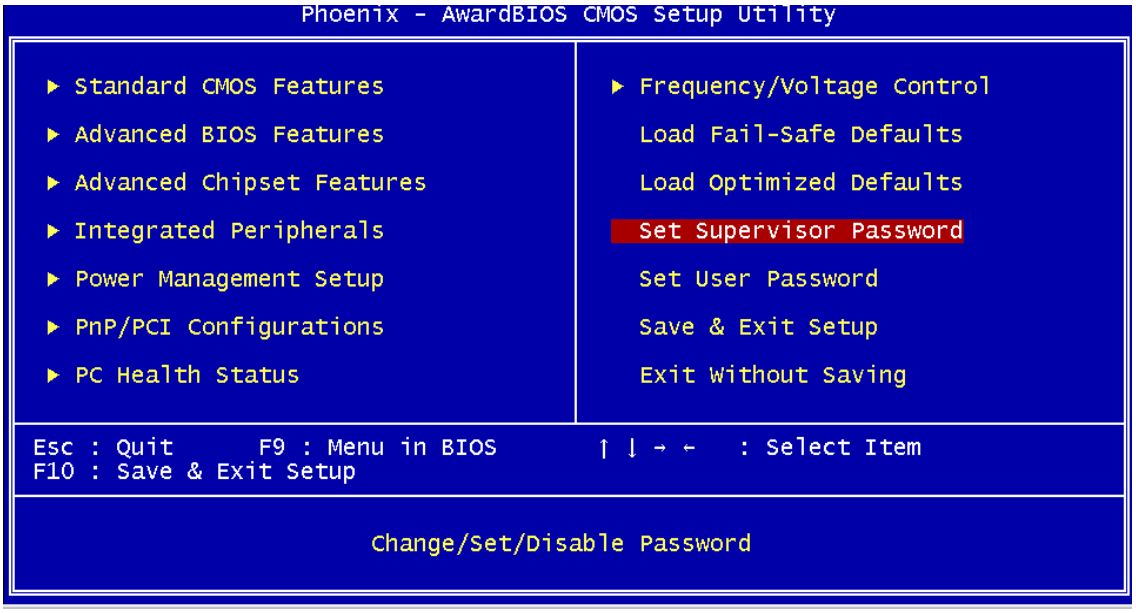
Pressing 'Y' loads the BIOS default values for the most stable, minimal-performance system operations.

4.5.11 Load Optimized Defaults

When you press <Enter> on this item you get a confirmation dialog box with a message similar to:

Pressing 'Y' loads the default values that are factory settings for optimal performance system operations.

4.5.12 Supervisor / User Password Setting



You can set either supervisor or user password, or both of them. The differences between are:

supervisor password: can enter and change the options of the setup menus.
user password: just can only enter but do not have the right to change the options of the setup menus. When you select this function, the following message will appear at the center of the screen to assist you in creating a password.

ENTER PASSWORD:

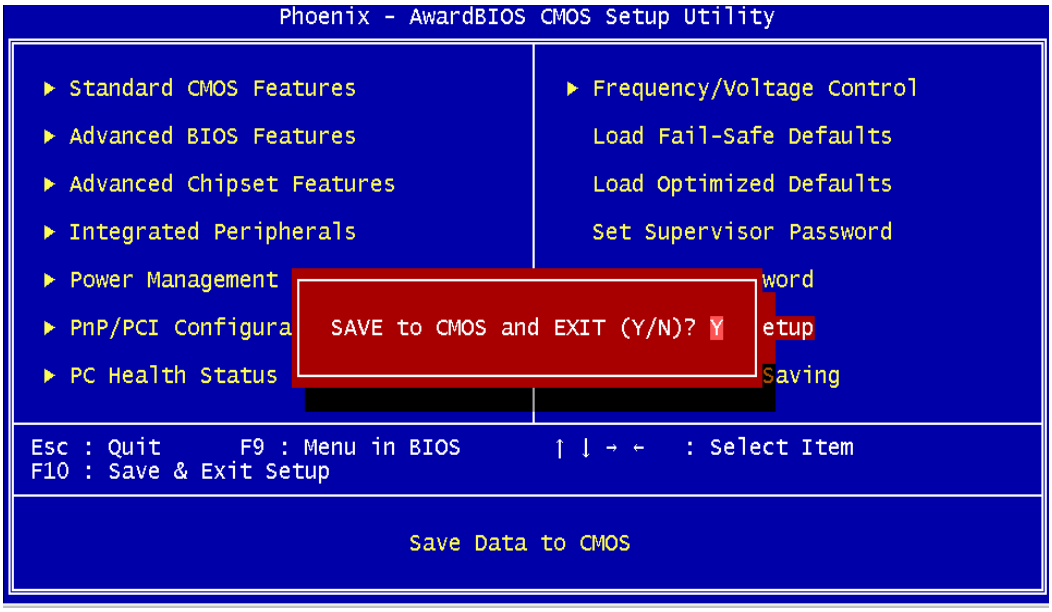
Type the password, up to eight characters in length, and press <Enter>. The password typed now will clear any previously entered password from CMOS memory. You will be asked to confirm the password. Type the password again and press <Enter>. You may also press <Esc> to abort the selection and not enter a password. To disable a password, just press <Enter> when you are prompted to enter the password. A message will confirm the password will be disabled. Once the password is disabled, the system will boot and you can enter Setup freely.

PASSWORD DISABLED.

When a password has been enabled, you will be prompted to enter it every time you try to enter Setup. This prevents an unauthorized person from changing any part of your system configuration. Additionally, when a password is enabled, you can also require the BIOS to request a password every time your system is rebooted. This would prevent unauthorized use of your computer. You determine when the password is required within the BIOS Features Setup Menu and its Security option (see Section 3). If the Security option is set to “System”, the password will be required both at boot and at entry to Setup. If set to “Setup”, prompting only occurs when trying to enter Setup.

4.5.13 Exit Selecting

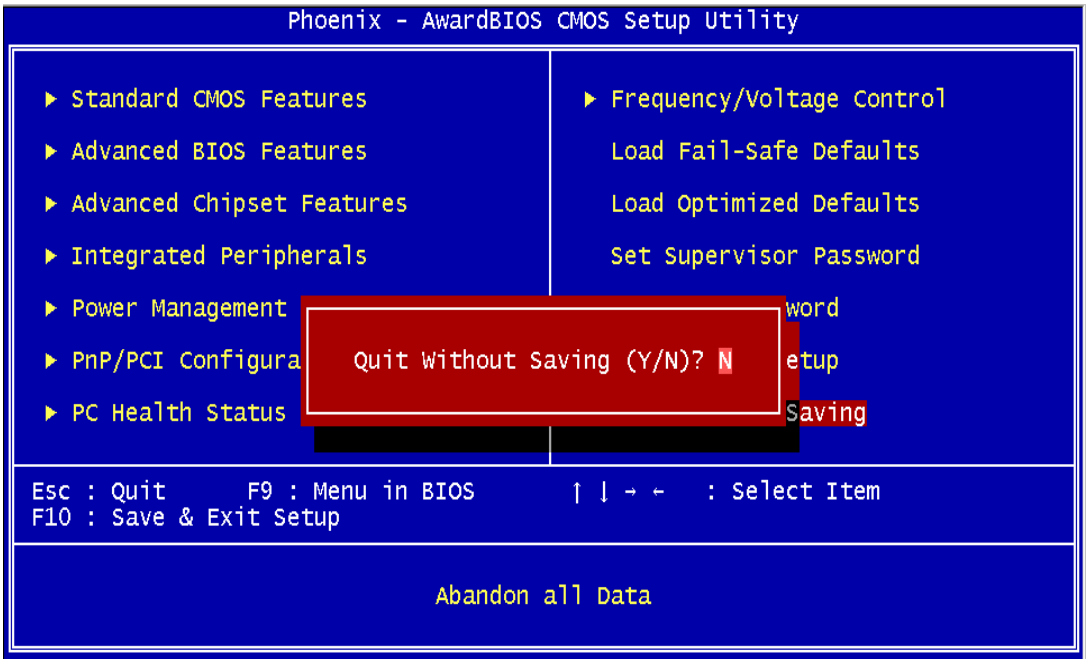
4.5.13.1 Save & Exit Setup



Pressing <Enter> on this item asks for confirmation:

Pressing "Y" stores the selections made in the menus in CMOS – a special section of memory that stays on after you turn your system off. The next time you boot your computer, the BIOS configures your system according to the Setup selections stored in CMOS. After saving the values the system is restarted again.

4.5.13.2 Exit Without Saving



Pressing <Enter> on this item asks for confirmation:

This allows you to exit Setup without storing in CMOS any change. The previous selections remain in effect. This exits the Setup utility and restarts your computer.

5. Driver Installation

5.1 Driver Installation for Ethernet Adapter

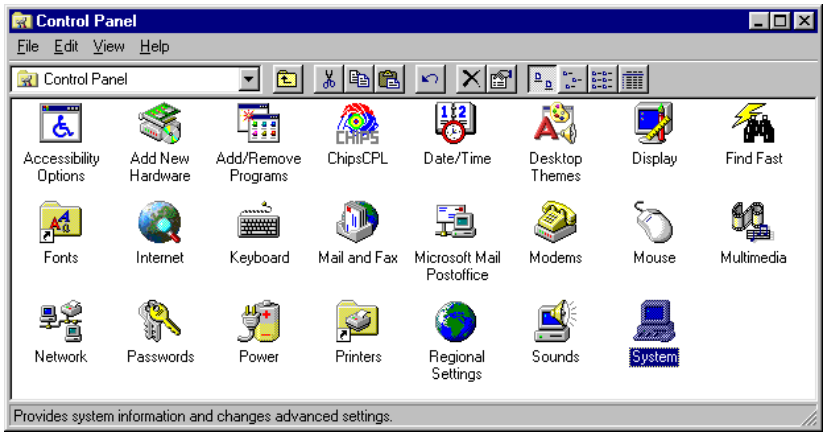
5.1.1 Windows 9x Ethernet Installation

The best way to install the driver for the Ethernet controller is to use the plug and play system of Windows 9x. The following procedures illustrate how the installation can be done.

1. If a driver for the Ethernet controller is already installed this must be removed first. This can be done by the following steps shown below.

   - Click the '*Start*' button, click on '*Settings*' and on '*Control panel*' to open the control panel.

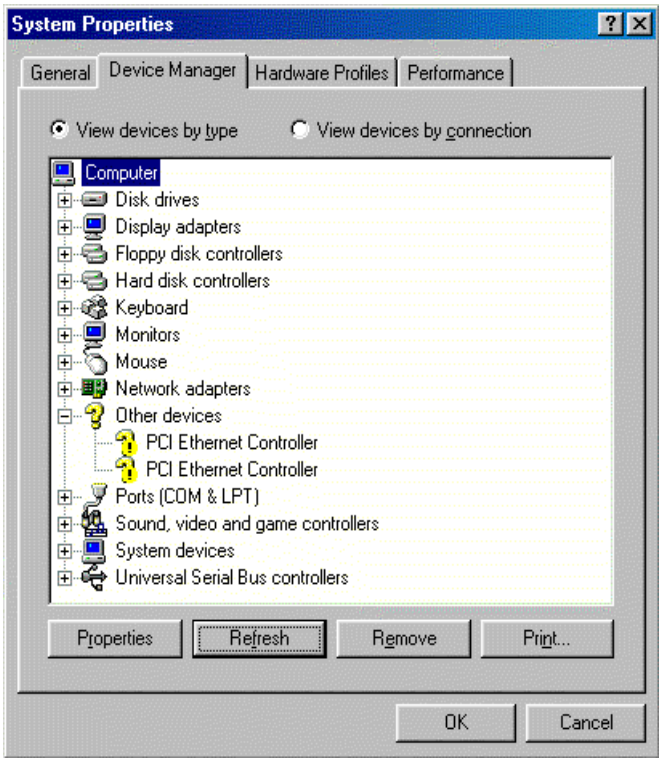
     Your display should now look as below (possibly with different size and icons):



   - Double click the '*System*' icon (highlighted above).
   - Select the '*Device Manager*' tab.

- If the '*Network adapters'* line is present, expand the line and remove the PCI Ethernet Controller adapters. This can be done by selecting the line and clicking the '*Remove'* button.

  Before removal of the adapter(s), your screen might look like this:



- When all adapters are removed (or none were present), a new driver can be installed.

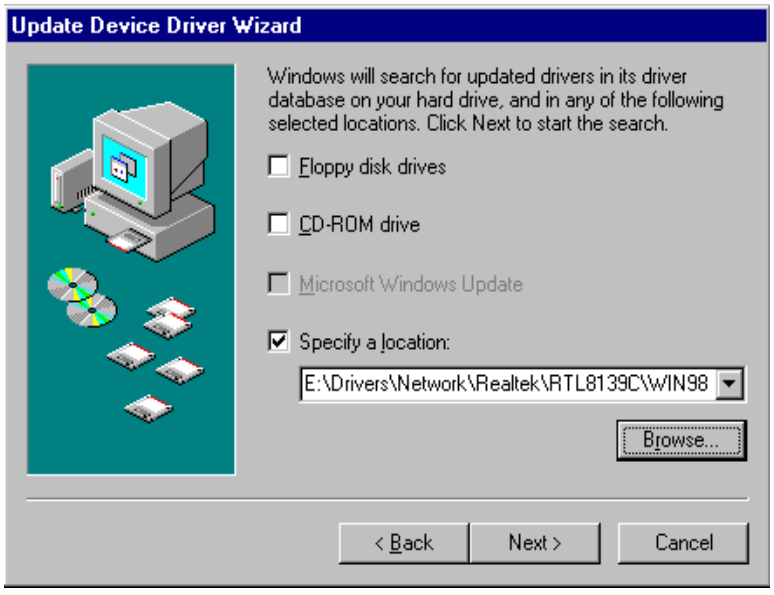
2. Reboot the computer.

3. During the boot the network adapter should be detected as shown below:

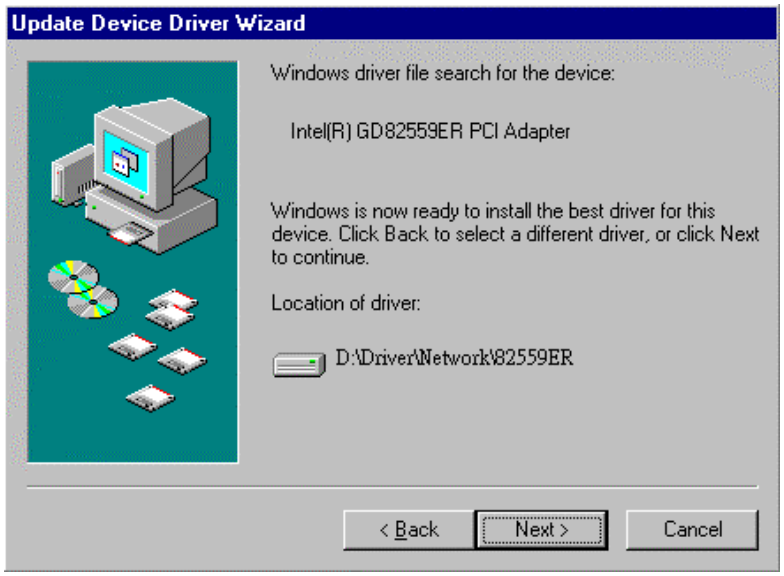
4. Specify the location of network adapter and click '*Next*' (see below).

.

If your CPU board using Realtek RTL8139C Network chip, the location of network adapter is shown as below.

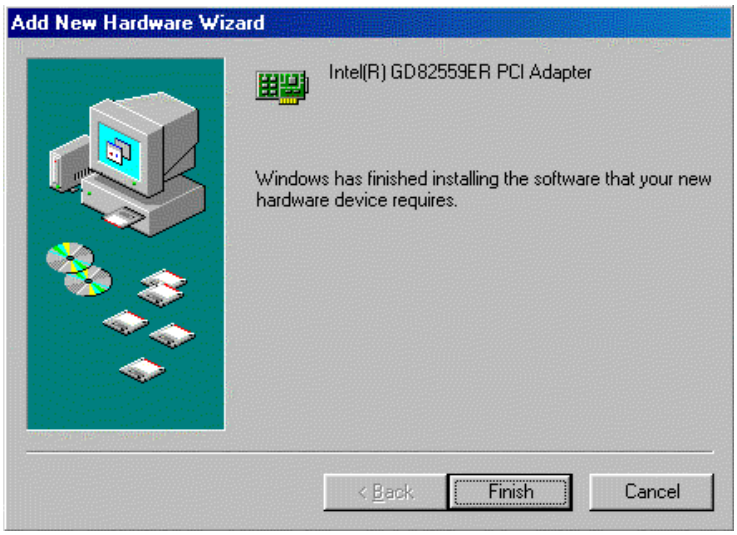


5. Click the '*Next*' button.

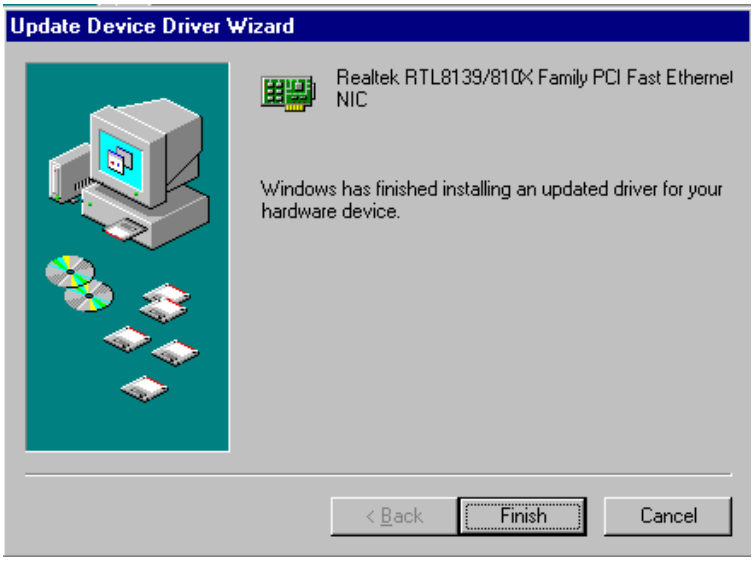


or

6. Click the '*Finish*' button.



or



7. Depending on the configuration, a request for the windows disks or CD-ROM may be necessary. Insert the disk / CD-ROM and click the '*OK*' button. An entry of the directory for the files may then be required. After typing the path name, click the '*OK*' button.

8. To complete the installation, reboot the computer by clicking the '*Yes*' button in the window shown below.

9. After the system restarts, the network adapter should be installed. Protocols, clients etc. may now be installed for the network in use.

Further configuration of the adapter may be made in the '*Advanced*' section of the driver properties. These options may be accessed through the '*Network*' icon in the control panel (Select the network adapter, click the '*Properties*' button and select the '*Advanced*' tab).

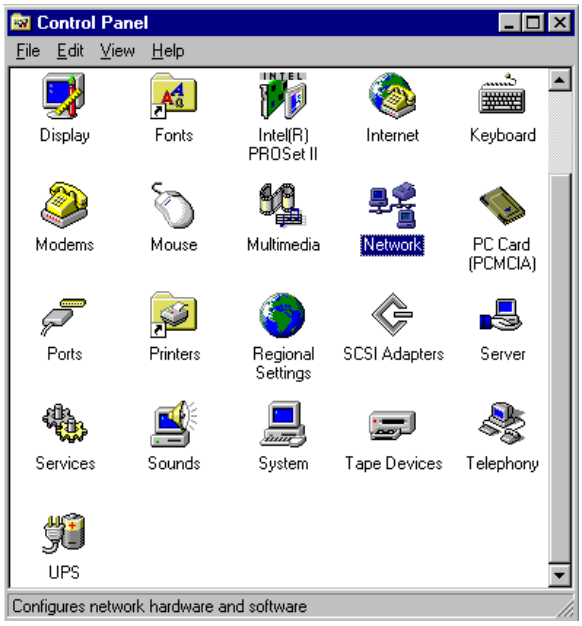
5.1.2 Windows NT 4.0 Ethernet Installation

A driver for the Intel 82559ER or Realtek RTL8139C Ethernet controller on board is included in the attached supporting CD-ROM. The driver for these adapters are denoted 'Intel GD82559ER PCI Adapter' or 'Realtek RTL8139(A/B/C) PCI Fast Ethernet Adapter'. The driver may be installed in two ways:

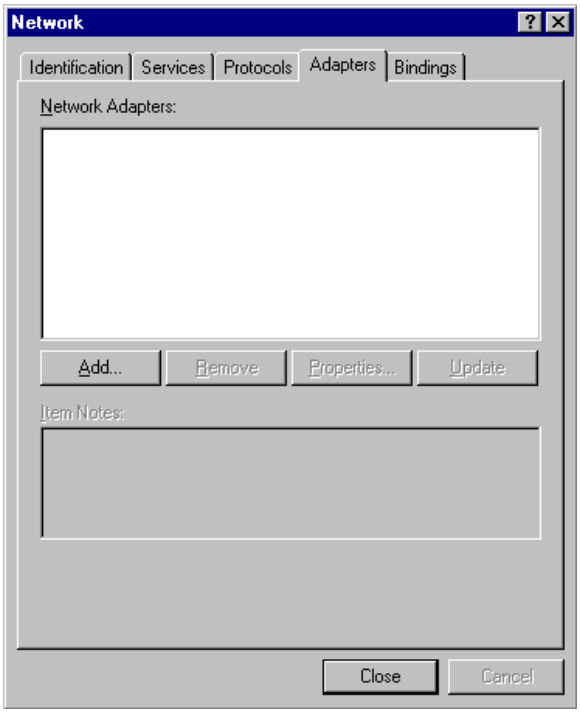
- During the installation process where the network may be configured as an integrated part. In this case the adapter may be chosen or auto-detected when the network adapter is to be installed.
- In the network settings after Windows NT 4.0 is installed.

The following procedures describe the steps to install the Network adapter driver on Windows NT 4.0.

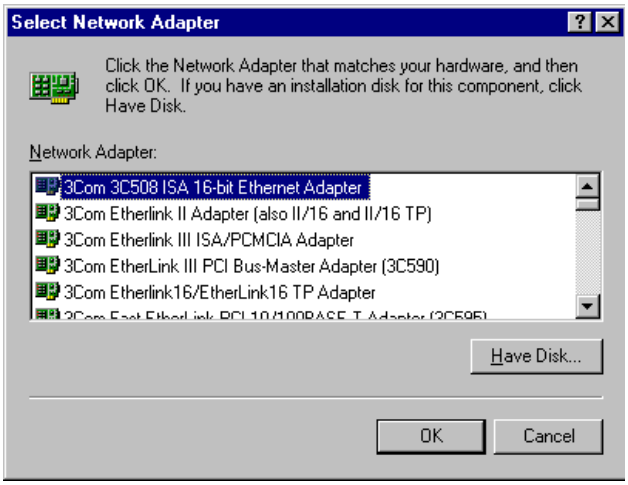
1. Click the '*Start'* button on the task bar. Select '*Settings'* and '*Control Panel'* to start the control panel shown below:



2. Double click the '*Network*' icon and then click the '*Adapters*' tab on the following window. A window as the one shown below should now appear.

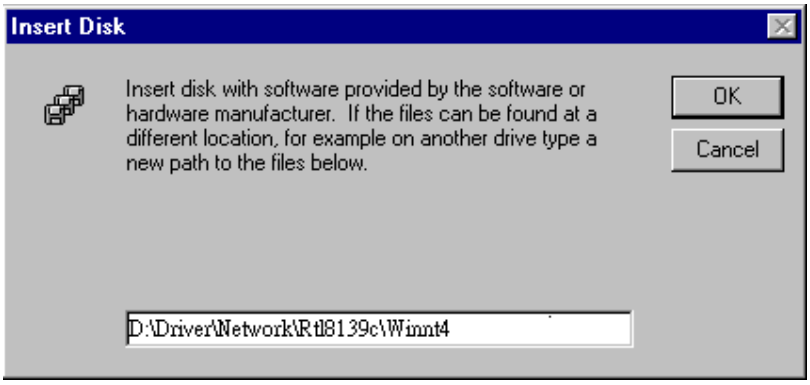


3. Click the '*Add...*' button, and the following window should appear.

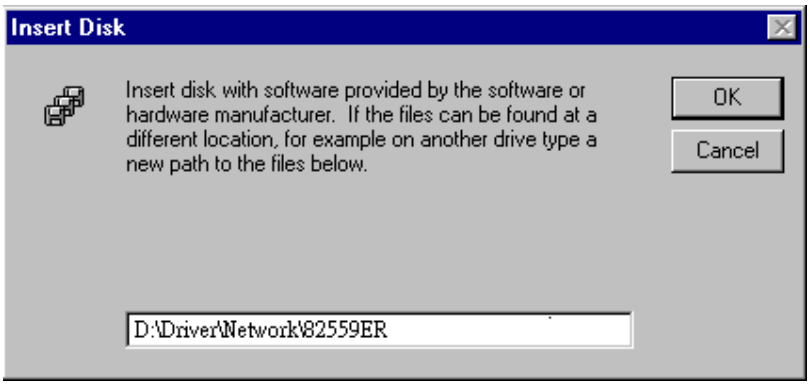


4. Click the '*Have Disk…*' button to install the Network adapter driver from CD-ROM. A window as the one shown below should now appear.

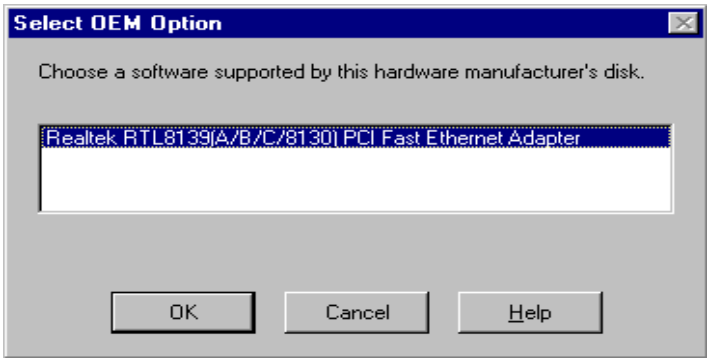
5. Locate the path of Network adapter driver and click the '*OK*' button.



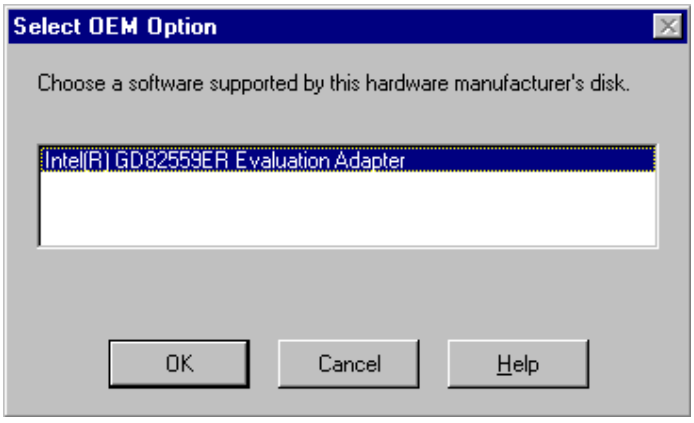
or



6. Select the '*Realtek RTL8139(A/B/C) PCI Fast Ethernet Adapter*' or '*Intel GD82559ER Ethernet Adapter*' from the list (as shown below) and click the '*OK*' button.

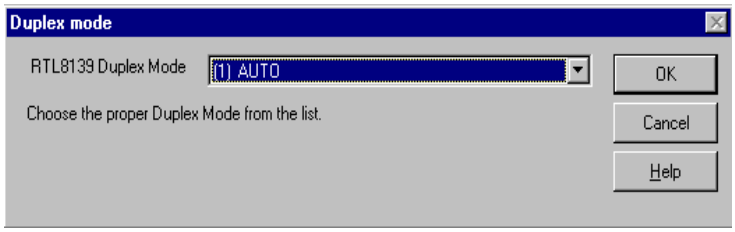


or

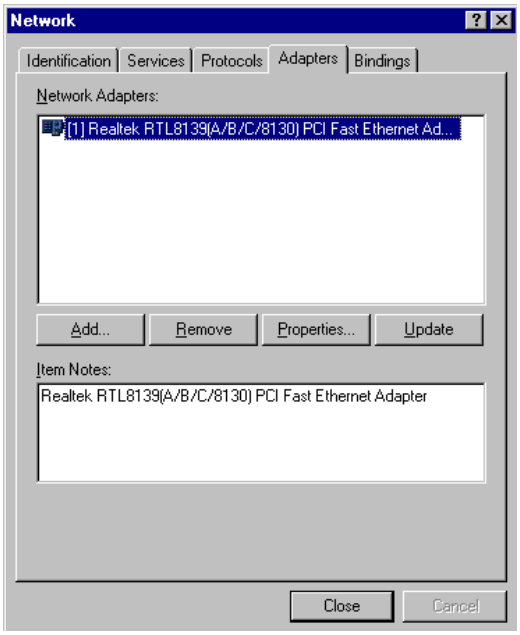


7. If your hardware using Intel-82559ER Ethernet controller, please proceed to 12.

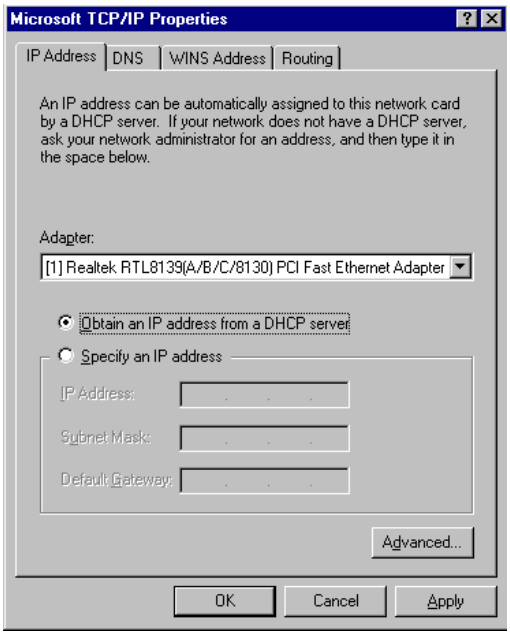
8. Select the '(1) Auto' to set RTL8139C Ethernet controller to Auto Duplex Mode (as shown below) and click the '*OK*' button.



9. Click '*Close*' to accept the settings.

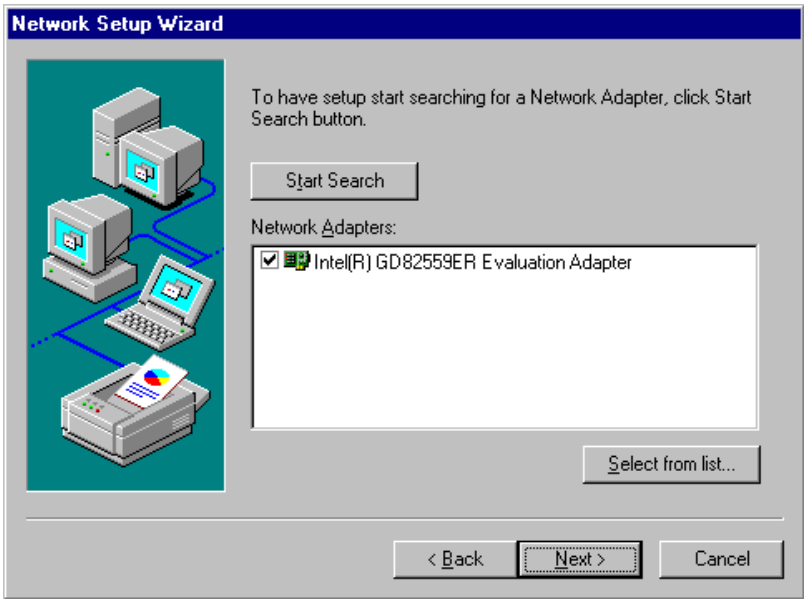


10. Protocols, Services etc. may now be installed and configured for the network to be used. An example is shown below.

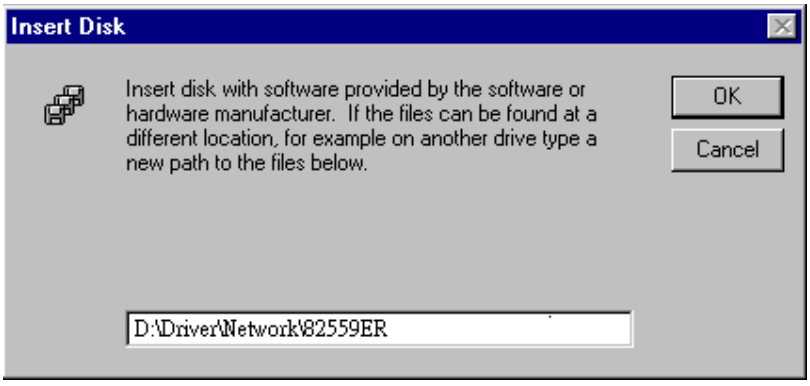


11. If your hardware using Realtek RTL8139C Ethernet controller, please proceed to 17.

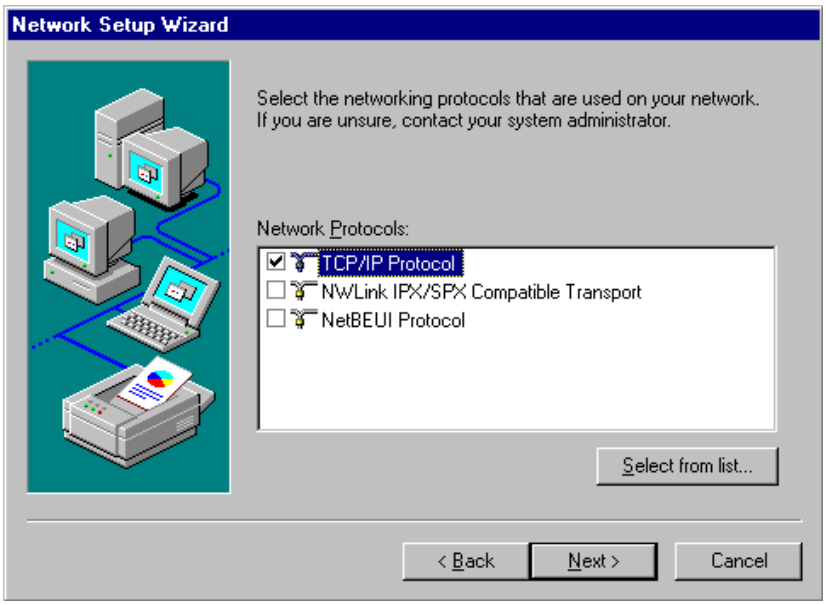
12. System will show as below.

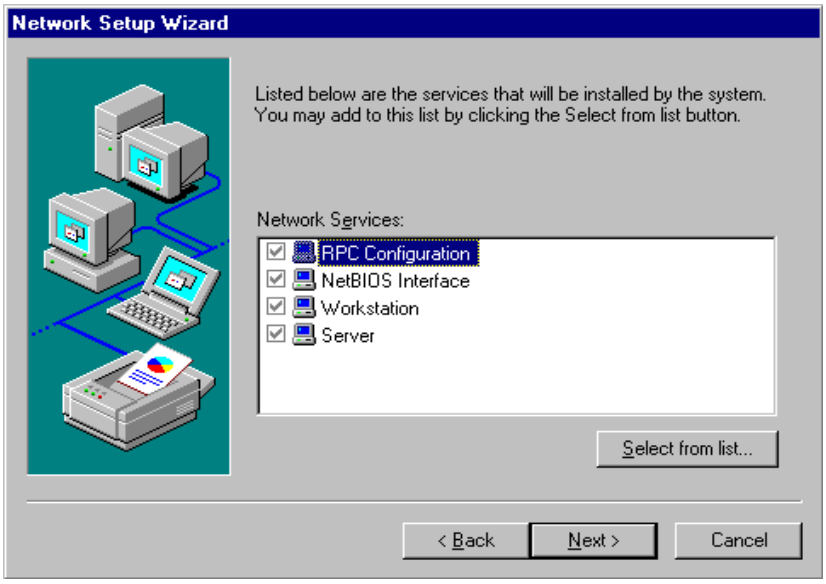


13. Files from your NT-distribution will now be needed. You may have to insert the CD-ROM and specify a directory of the files. An example is shown below.

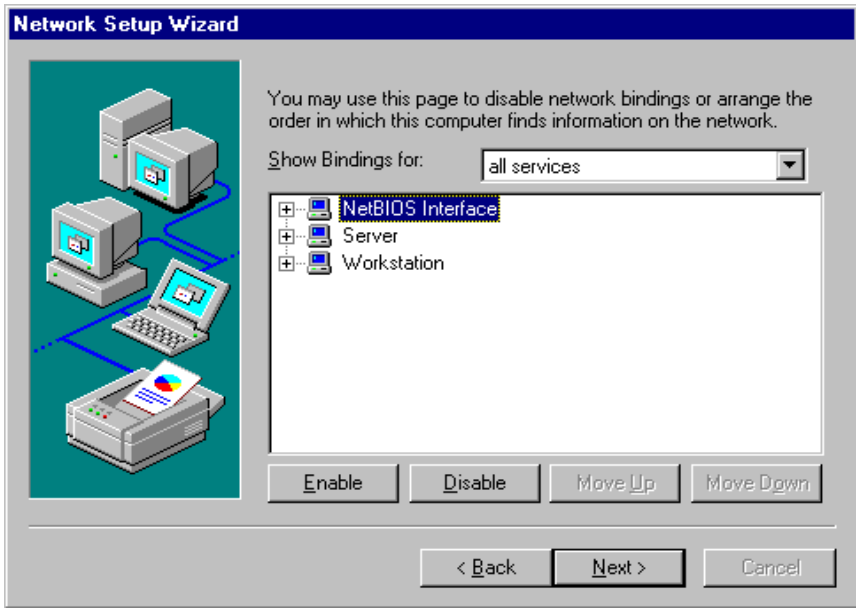


14. Protocols, Services etc. may now be installed and configured for the network to be used. An example is shown below.

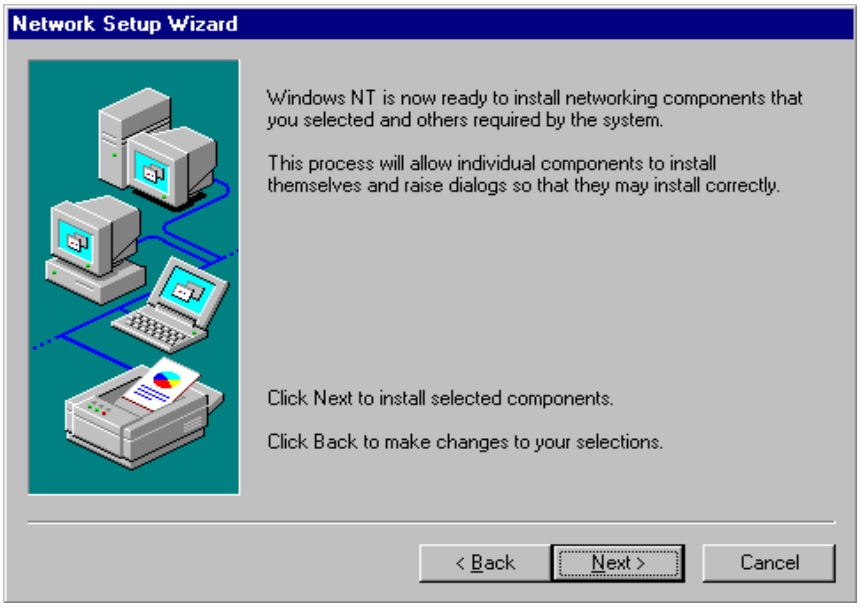




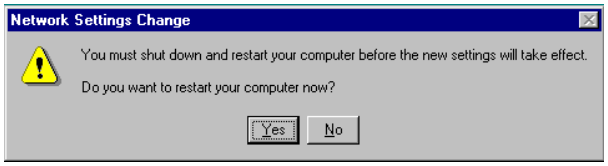
15. Click '*Next*' to accept the settings.



16. Click '*Next*' button. The network driver should now be installed.



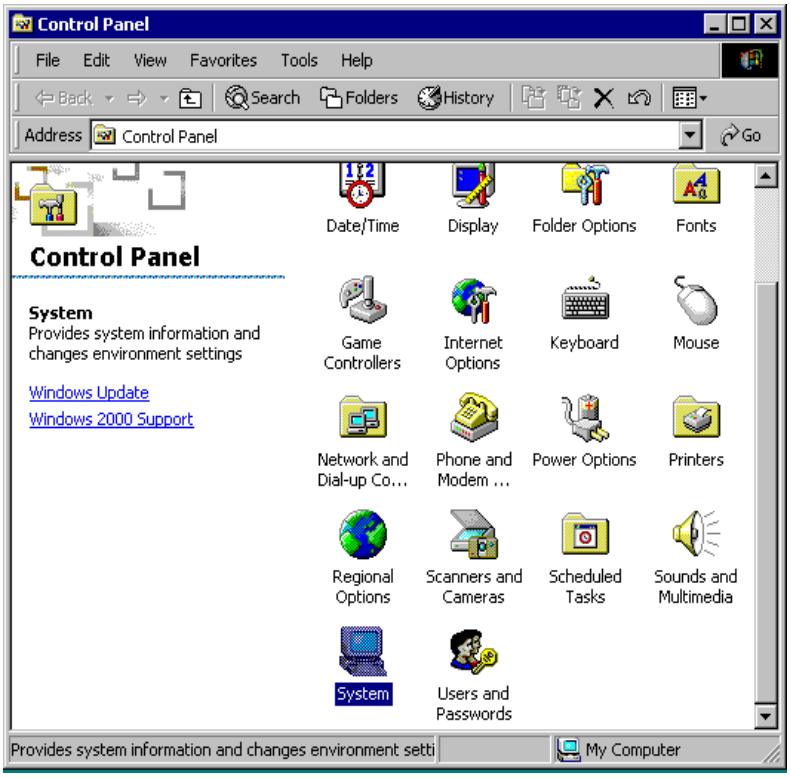
17. To complete the installation, reboot the computer by clicking the '*Yes*' button in the window shown below.



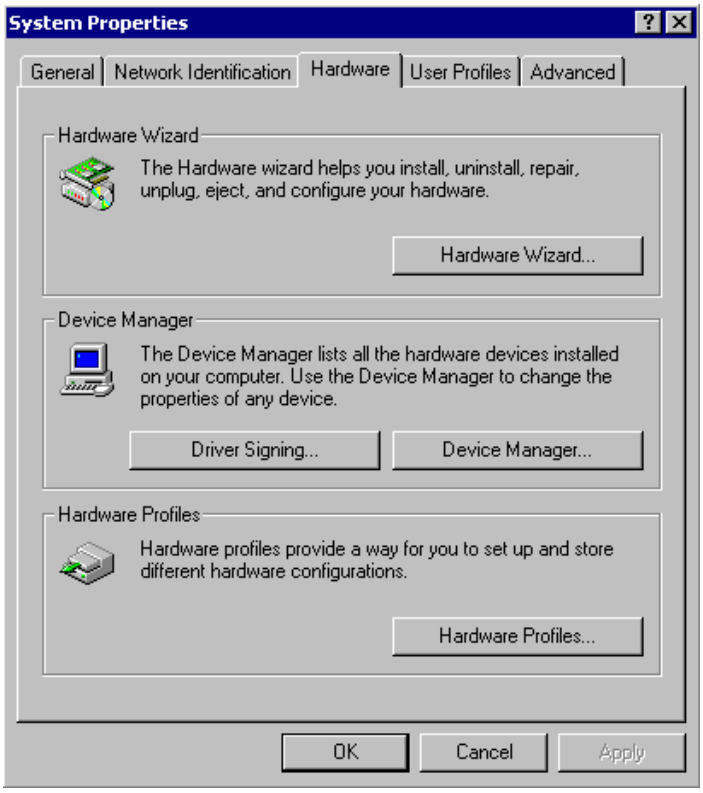
5.1.3 Windows 2000 Ethernet Installation

A driver for the Intel GD82559ER or Realtek RTL8139C PCI Fast Ethernet controller on board is included in the attached supporting CD-ROM. The driver for this adapter is denoted ’Intel GD82559ER PCI Adapter’’ or ’Realtek RTL8139(A/B/C) PCI Fast Ethernet Adapter’.

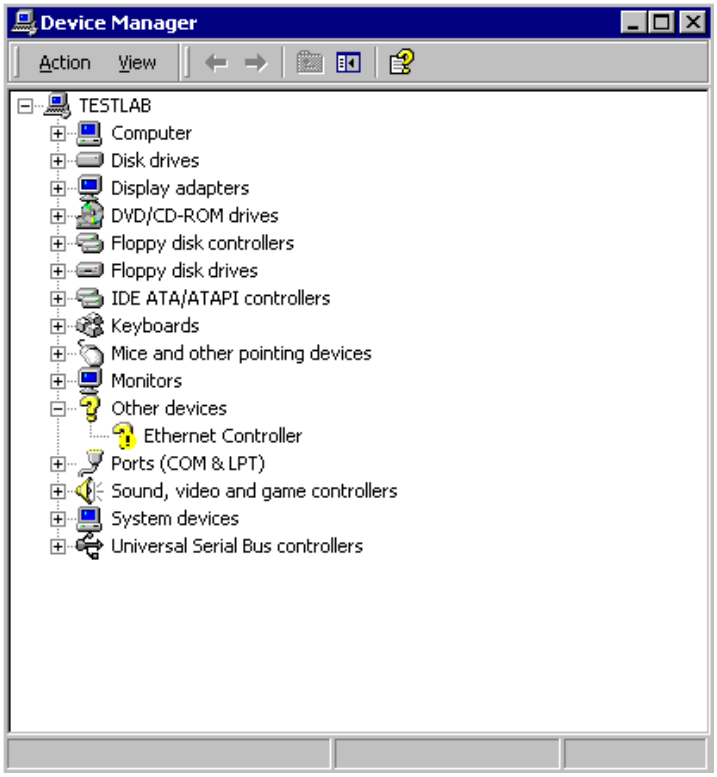
1. Start the control panel by clicking the ‘*Start*’ button, click‘*Settings*’ and ‘*Control Panel*’ from the sub-menu. Double click the ‘System’ icon in the control panel as shown below.



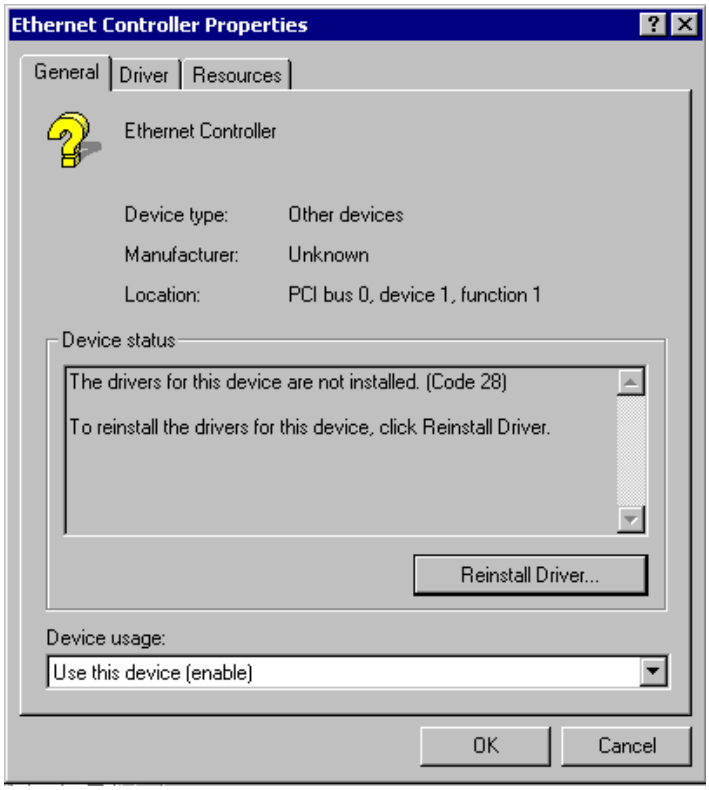
2. On the System properties window, click the *'Hardware'* tab as shown below.



3. Click the *'Device Manager…'* button to show the Device Manager.



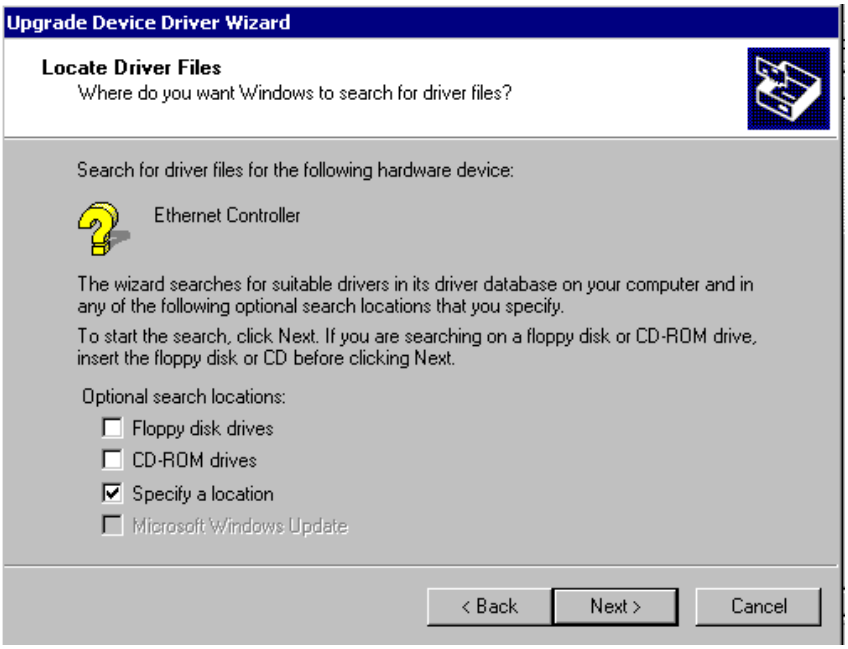
4. Double click *'Ethernet Controller'*. This will show the following window. Click the '*Reinstall Driver'* button.



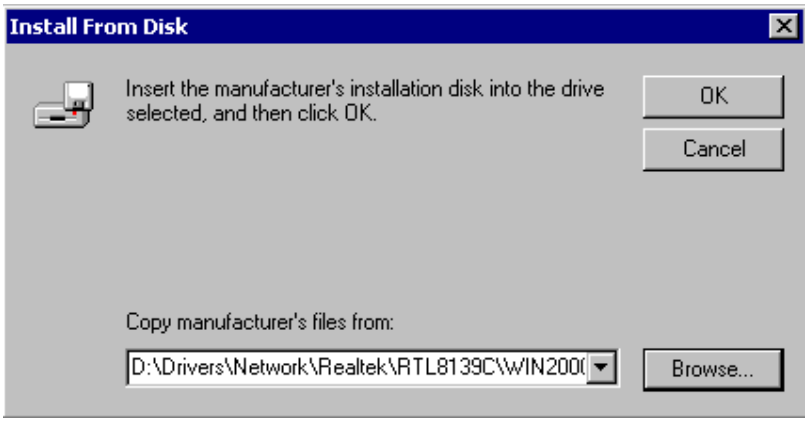
5. Click the '*Next*' button to run upgrade device driver wizard.

6. Click the *'Next'* button to continue the driver installation.

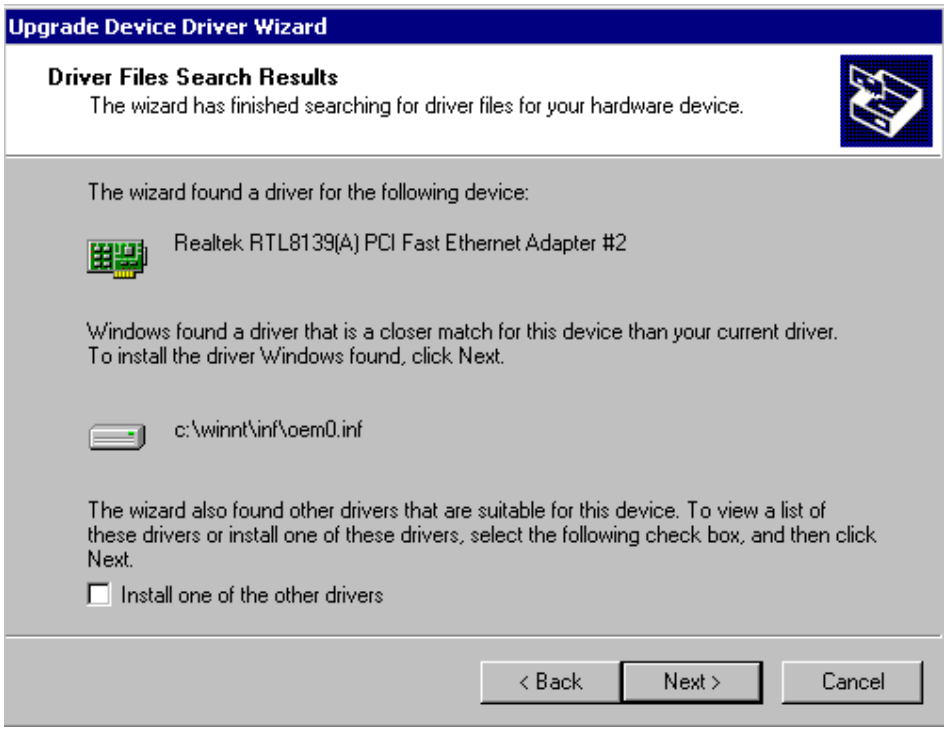
7. Select the *'Specify a location'* check item, click the *'Next'* button to continue.



8. The directory for the drivers may now be entered or click the *'Browse…'* button to select the directory. Click the *'OK'* button to continue.

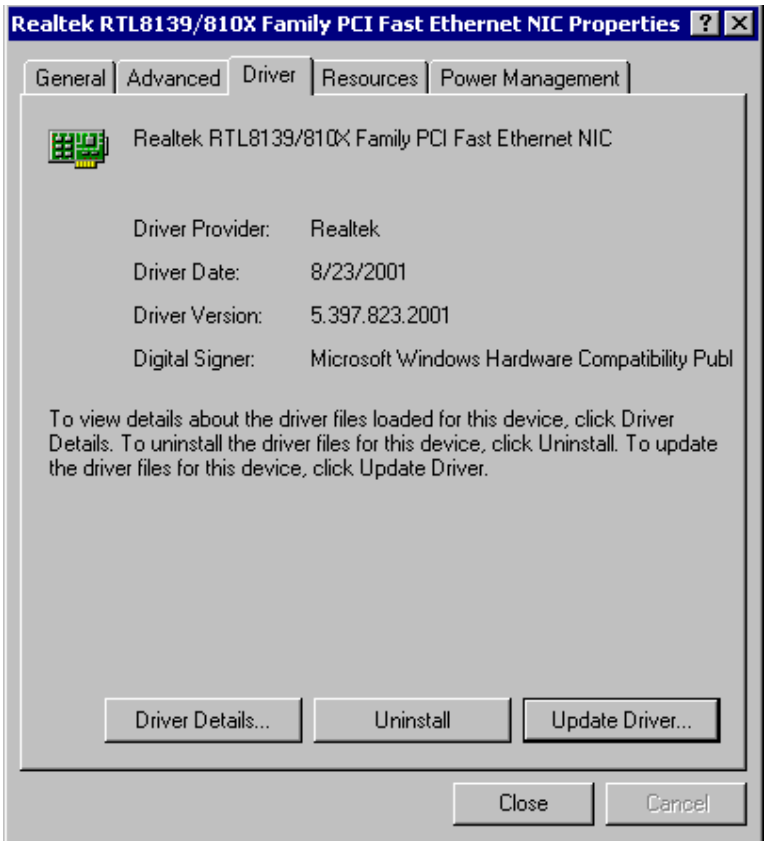


9. After system search the driver, click the *'Next'* button to continue the driver upgrade.



10. After driver has been installed to system, the follow windows should appear, click the *'Finish'* button to finish the driver installation.

11. After finish the driver installation, system will return to Properties windows as shown below. Click the ‘Close’ button to return the Device Manager.



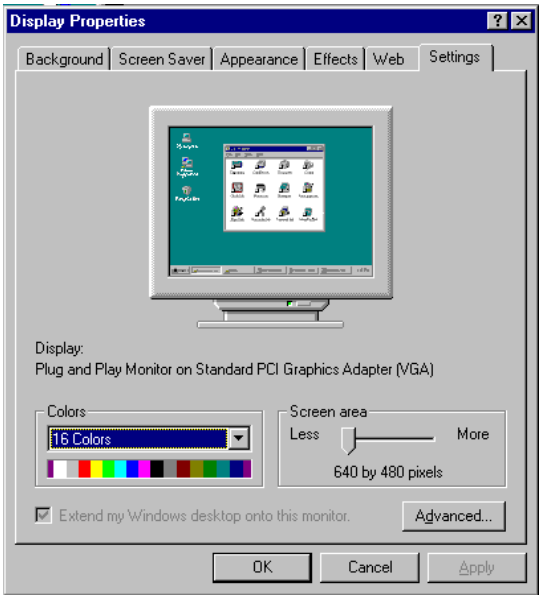
5.2 Driver Installation for Display Adapter

5.2.1 Windows 9x

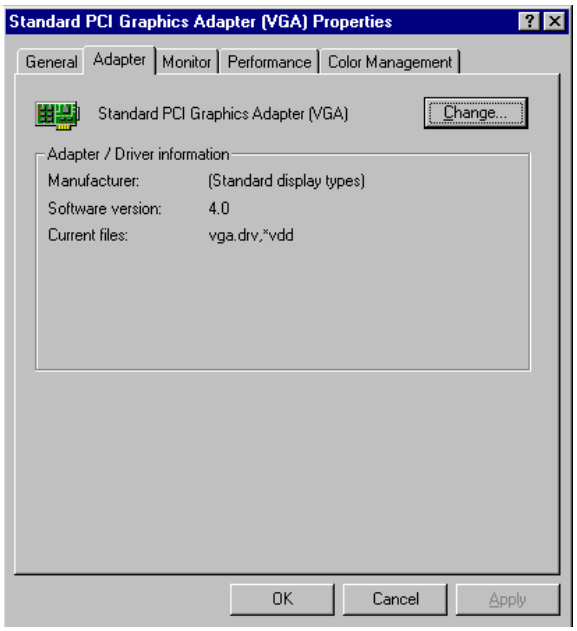
The following steps will install the display driver for the S3-TwisterT display controller.

1. Click the '*Start*' button on the task bar, select '*Settings*' and '*Control Panel*' from the sub-menu. This should start the Control Panel as shown below:

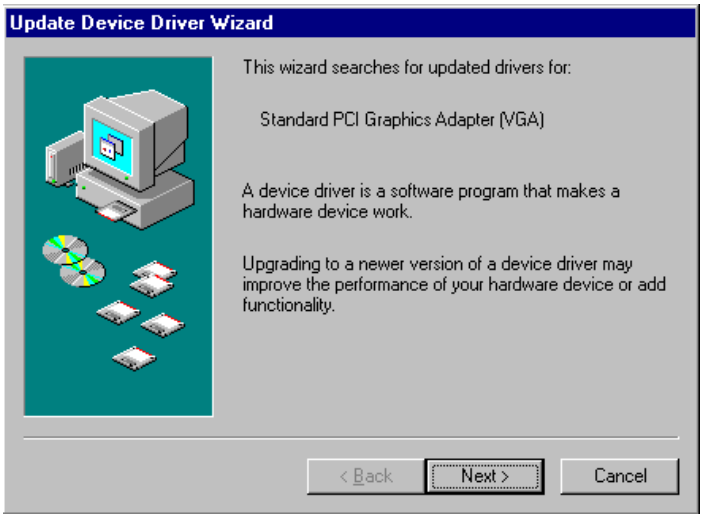
2. Double click the '*Display*' icon and select the '*Settings*' tab as shown below.



3. Click the '*Advanced…*' button. This will show the following window. Click the '*Change…*' button in the Adapter Type frame to select another driver. Your display will probably have another driver then the 'Standard PCI Graphics Adapter (VGA)' installed at this moment.

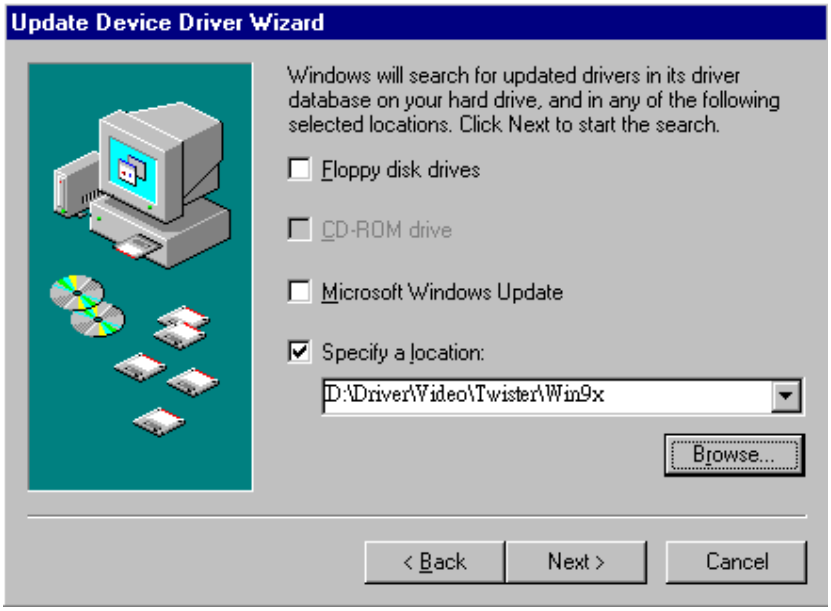


4. Click the '*Next*' to update the display driver.

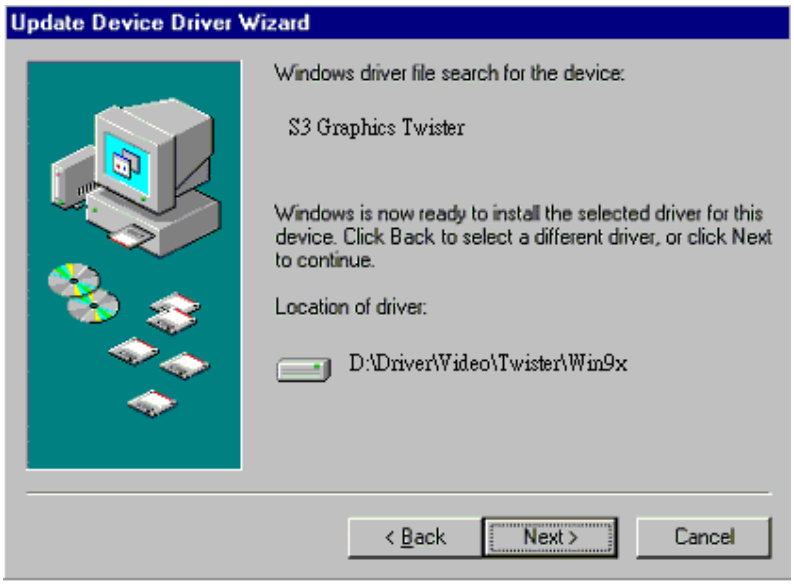


5. Click the '*Next*' to continue the display driver installation.

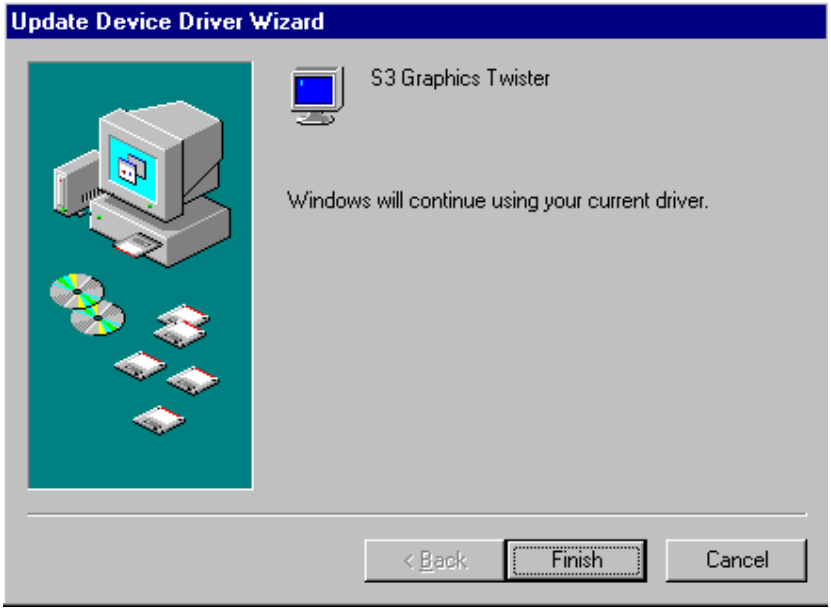
6. Locate the path of Graphics adapter driver and click the '*Next*' button.



7. The driver files will now be read and the display adapter is shown as the following. Click the '*Next*' button to install the display driver.



8. Click the '*Finish*' button.



9. To complete the display driver installation, reboot the computer by clicking the '*Yes*' button in the window shown below.

10. Further configuration of the display adapter may be made from the '*Display Properties*' window (follow step 1 above). The '*Settings*' tab allows you to change resolution, number of colours etc.

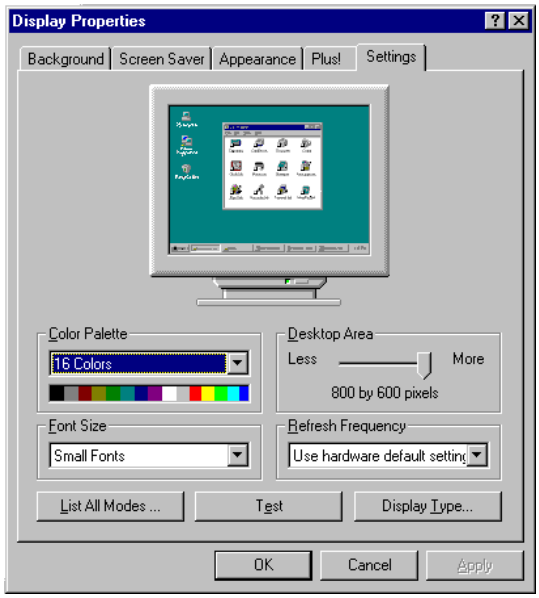
5.2.2 Windows NT 4.0 Display Installation

A display driver for Windows NT 4.0 is supplied with the system on the supporting CD-ROM.

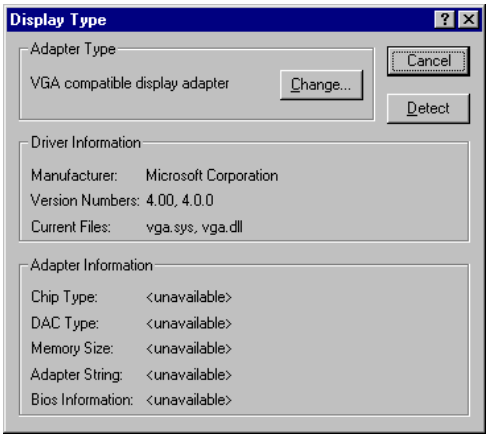
The driver installation may be performed by following steps shown below:

1. Start the control panel by clicking the '*Start*' button, click '*Settings*' and '*Control Panel*' from the sub-menu. Double click the '*Display*' icon in the control panel as shown below.

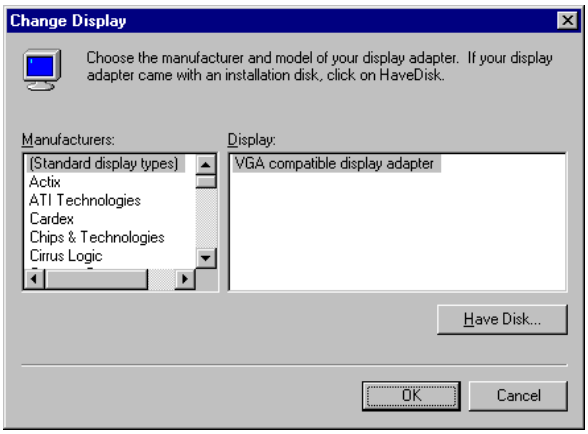
2. On the Display properties window, click the '*Settings*' tab as shown below.



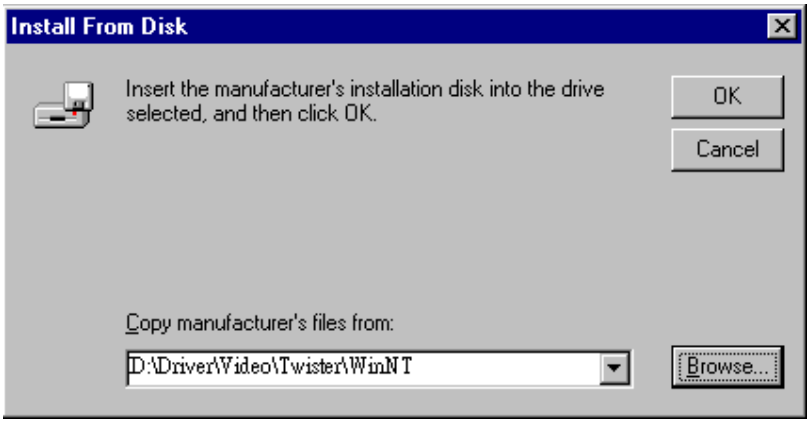
3. Click the '*Display Type…*' button and the following window should appear. Click the '*Change…*' button to select another driver.



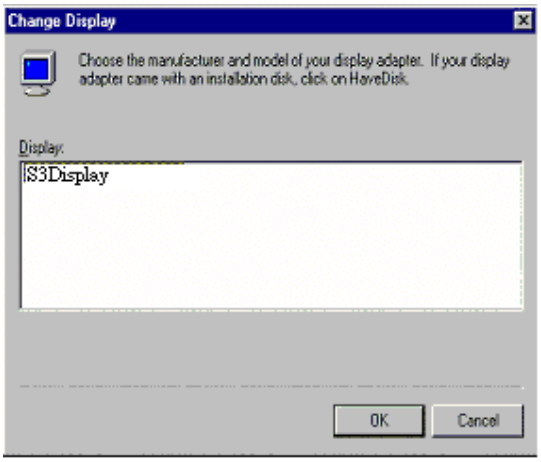
4. Click the '*Have Disk…*' button.



5. The directory for the drivers may now be entered. Type D:\Drivers\Video\Twister\winnt as shown below. Insert the '*Display driver disk*' and click '*OK*'.

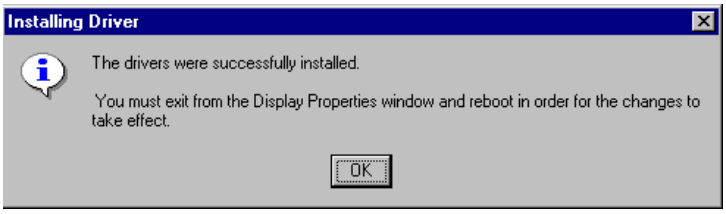


6. The display driver should now be listed as shown below. Click '*OK*' to accept.



7. Since this driver is not part of the NT4.0 package, the following message will be shown.

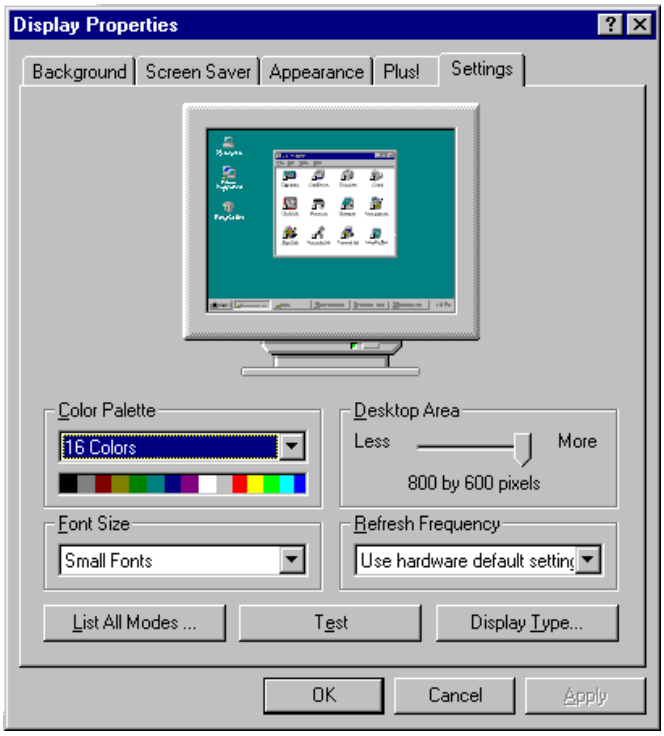
8. To proceed the driver installation, click the '*Yes*' button. The driver will now be installed, and the following message should be shown shortly.



9. Click '*OK*' and close the '*Display Type*' and '*Display Properties*' windows by clicking the '*Close*' button in each window.

10. After closing the '*Display Properties*' window, the computer must be restarted for the changes to take effect.

11. After the reboot, display resolution etc. may be configured in the '*Display Properties*' window (opened by following steps 1 and 2 shown above). An example is shown below.



12. Before accepting the new settings by pressing '*OK*', a test should be performed by clicking the '*Test*' button.

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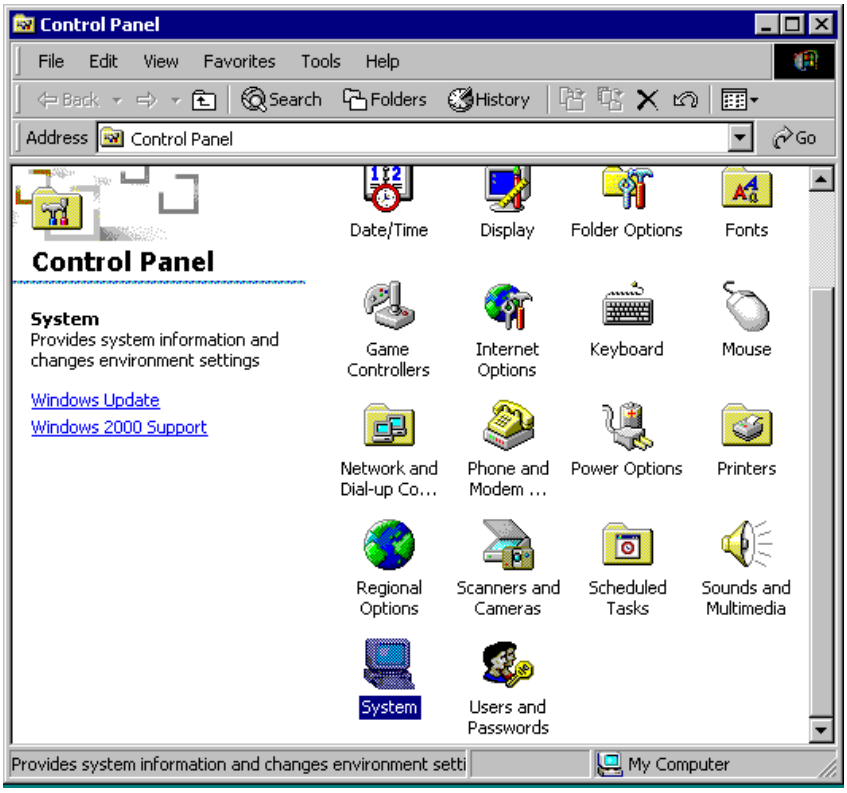
5.2.3 Windows 2000 Display Installation

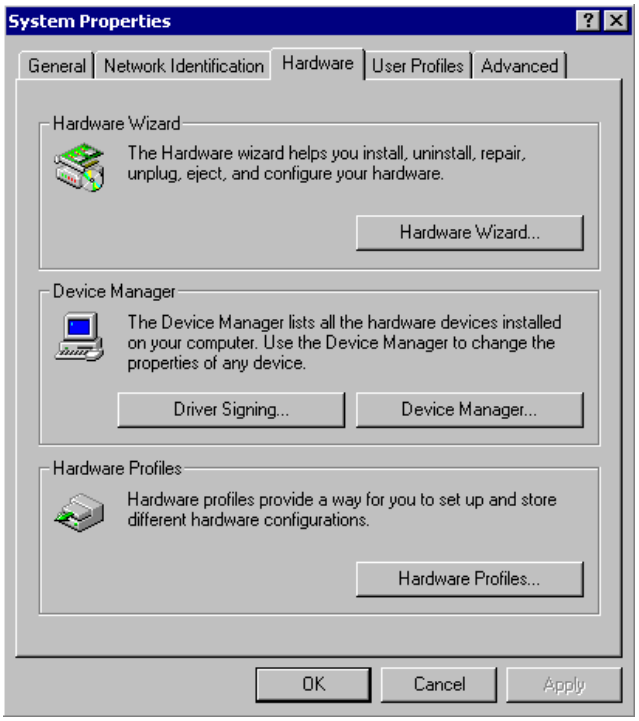
A display driver for Windows 2000 is supplied with the system on the supporting CD-ROM.

The driver installation may be performed by following steps shown below:

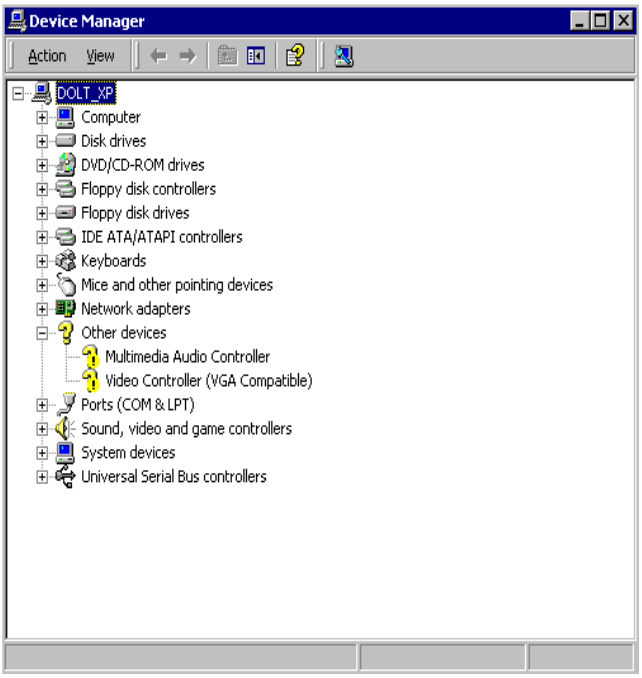
1. Start the control panel by clicking the '*Start*' button, click '*Settings*' and '*Control Panel*' from the sub-menu. Double click the 'System' icon in the control panel as shown below.



2. On the System properties window, click the 'Hardware' tab as shown below.



3. Click the 'Device Manager…' button to show the Device Manager.

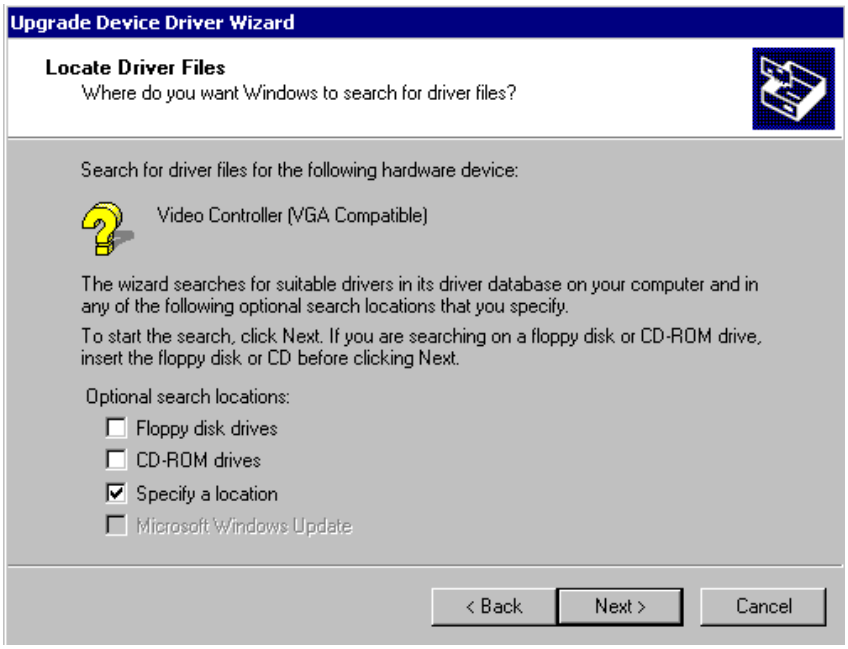


4. Double click ‘Video Controller (VGA Compatible)’. This will show the following window. Click the ‘*Reinstall Driver’* button.

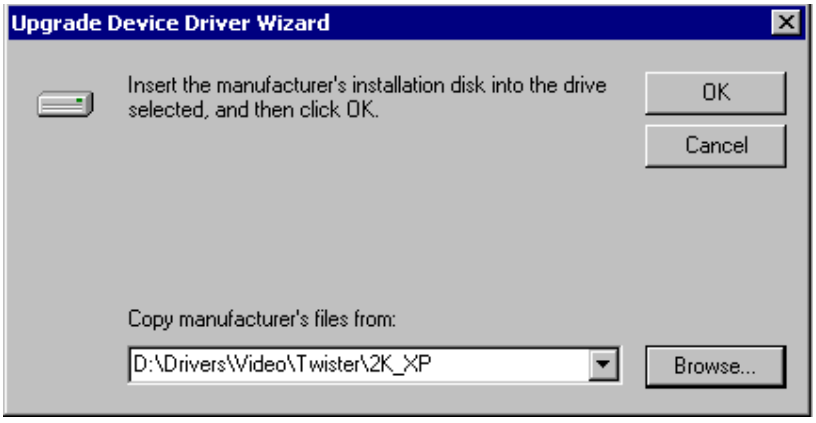
5. Click the '*Next*' button to run upgrade device driver wizard.

6. Click the *'Next'* button to continue the video driver installation.

7. Select the *'Specify a location'* check item, click the *'Next'* button to continue.



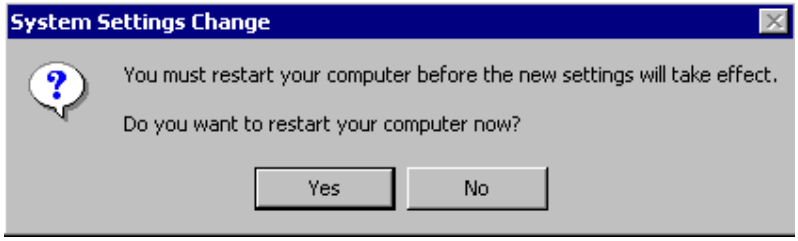
8. The directory for the drivers may now be entered or click the *'Browse…'* button to select the directory. Click the *'OK'* button to continue.



9. After system search the driver, click the *'Next'* button to continue upgrade driver.

10. After the driver has been installed to system, the follow windows should appear, click the *'Finish'* button to finish the driver installation.

11. To complete the driver installation, reboot the computer by clicking the '*Yes*' button in the window shown below.

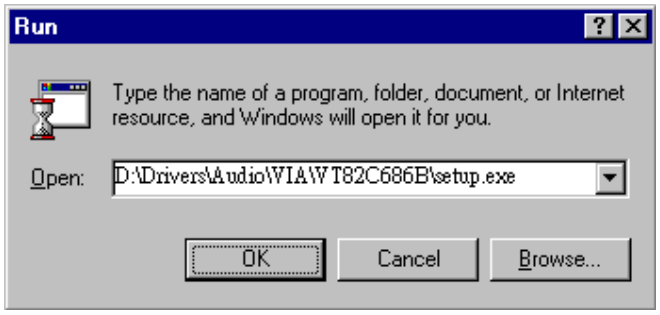


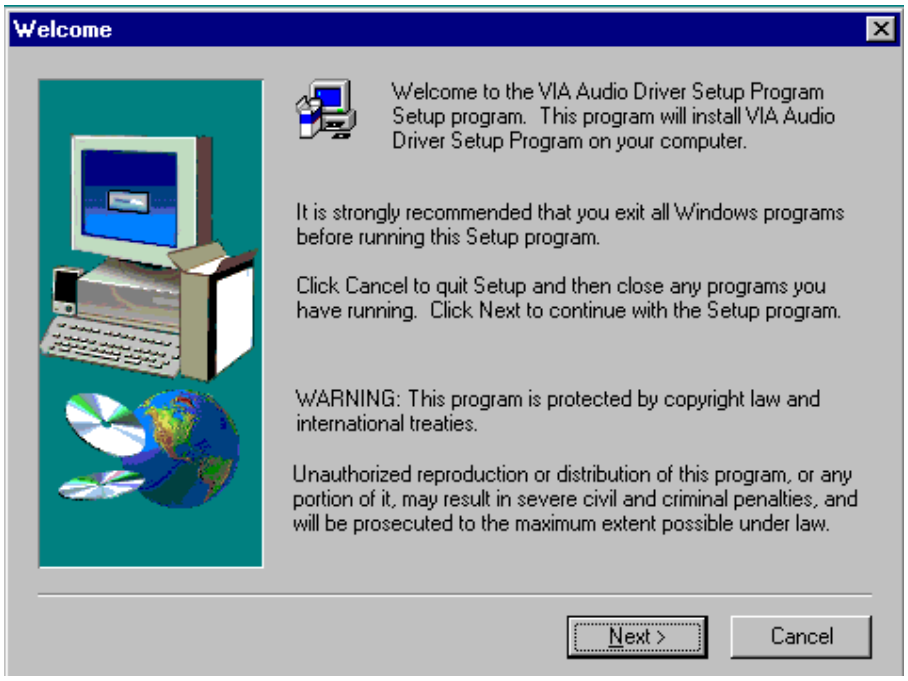
5.3 Driver Installation for Audio Adapter

5.3.1 Windows 9x

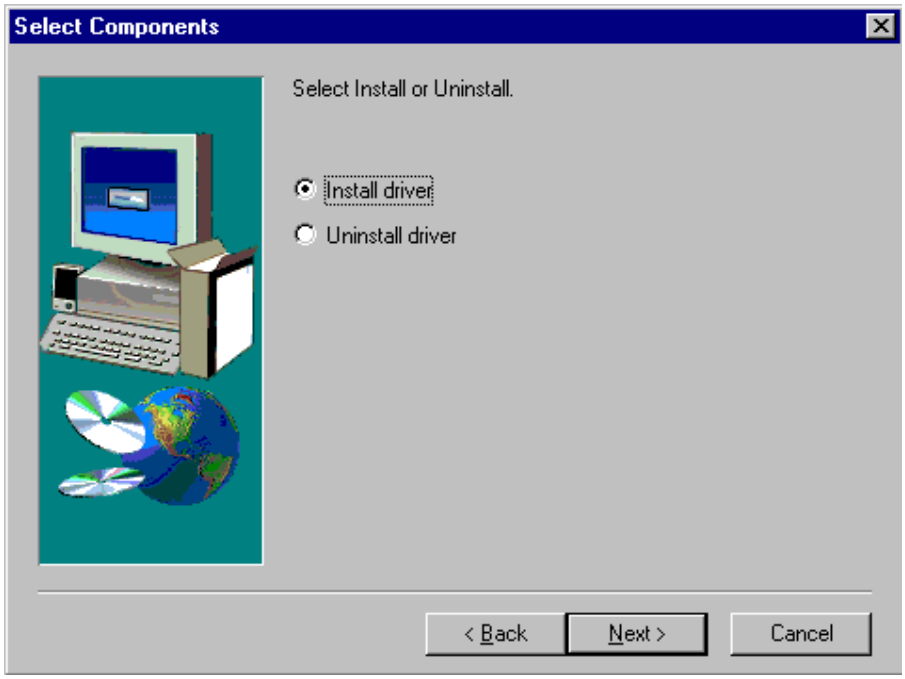
The following steps show how to install the VIA AC97 audio driver.

1. Click the '*Start*' button on the task bar, select '*Run*' and specify the location of VIA AC97 Audio driver setup program. This should start the VIA AC97 Audio driver setup program as shown below:

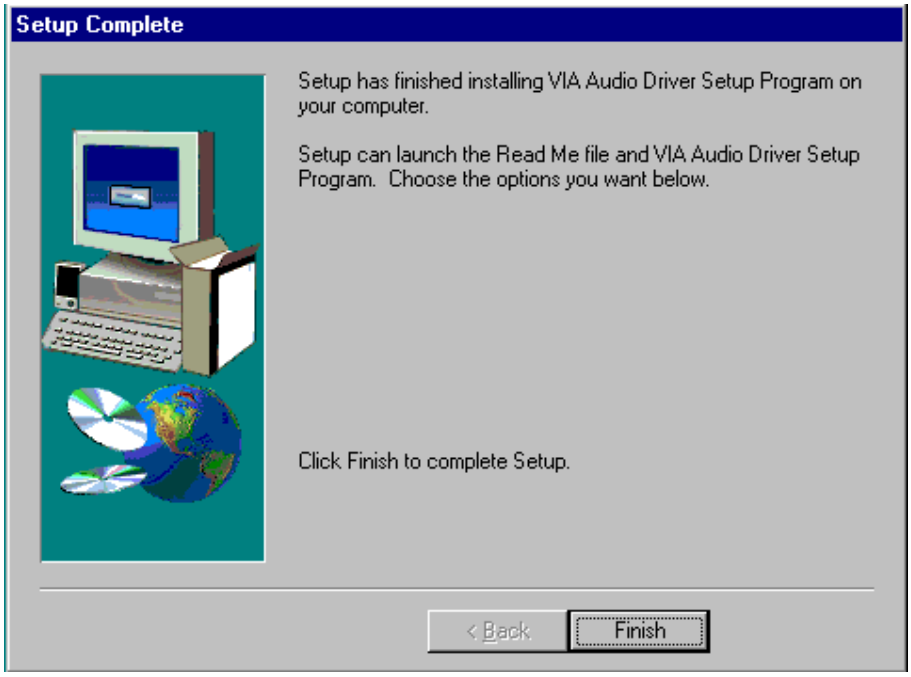




2. Select '*Install driver*' as shown below.



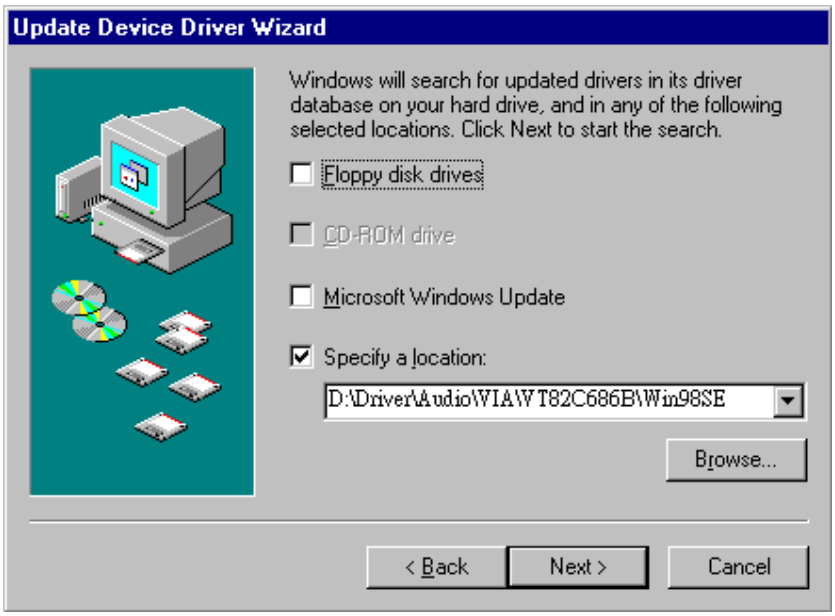
3. Click the '*Finish*' button to complete the driver setup.



4. Click the '*Next*' to update the audio driver.

5. Click the '*Next*' to continue the audio driver installation.

6. Locate the path of Audio adapter driver and click the '*Next*' button.



7. The driver files will now be read and the audio adapter is shown as the following. Click the '*Next*' button to install the audio driver.

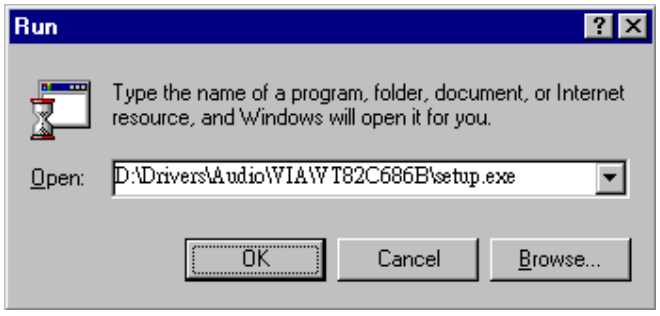
8. Click the '*Finish*' button to complete the display driver installation.

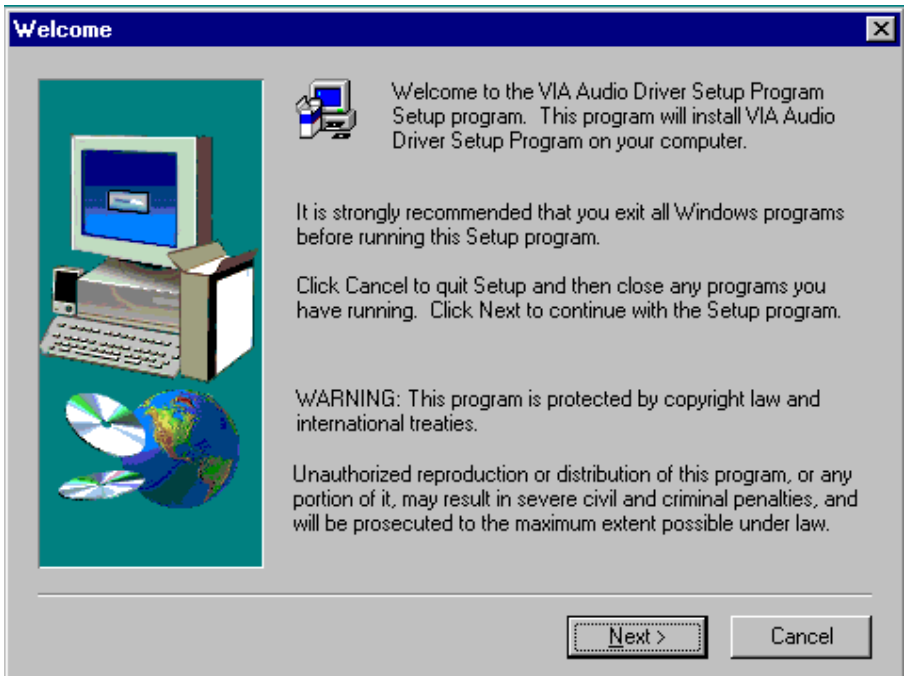
5.3.2 Windows NT 4.0 Audio Installation

An audio driver for Windows NT 4.0 is supplied with the system on the supporting CD-ROM.

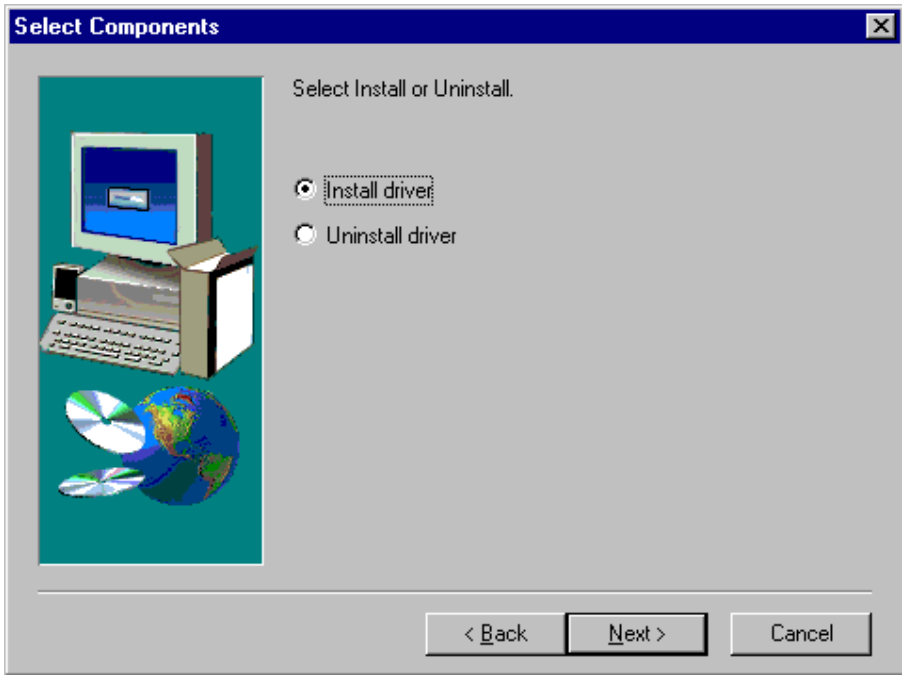
The driver installation may be performed by the following steps:

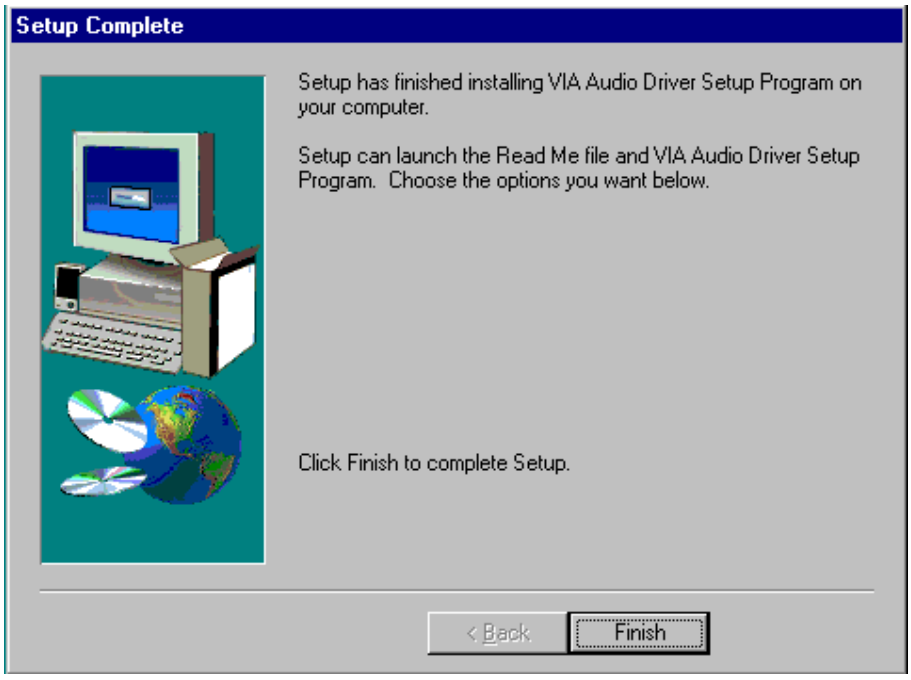
1. Click the '*Start*' button on the task bar, select '*Run*' and specify the location of VIA AC97 Audio driver setup program.This should start the VIA AC97 Audio driver setup program as shown below:



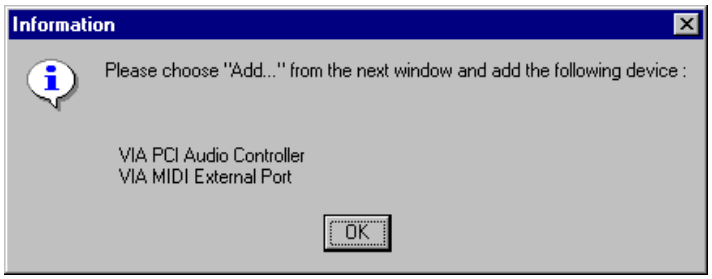


2. Select '*Install driver*' as shown below.

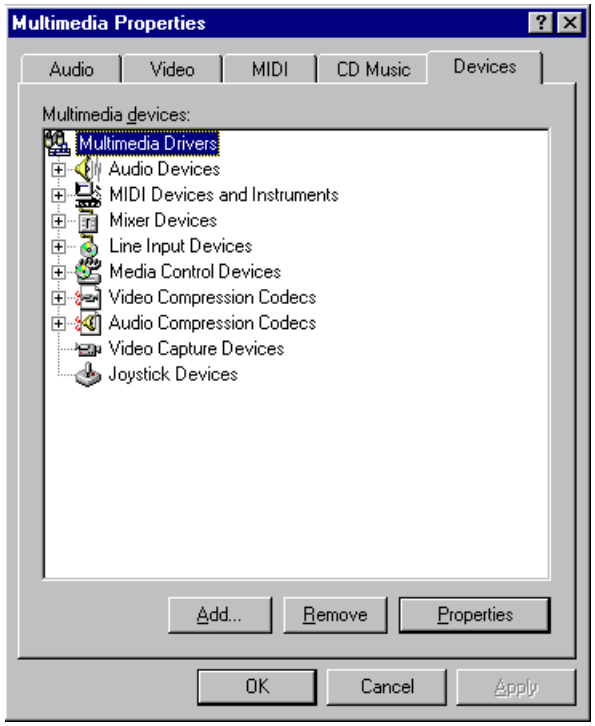




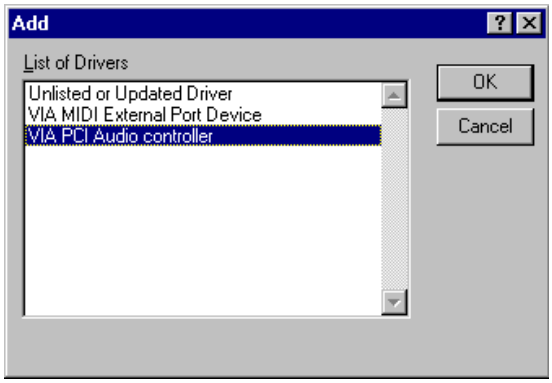
3. Select '*OK*' as shown below.



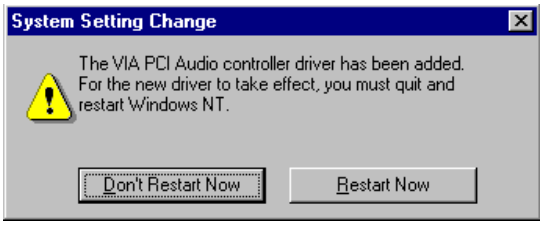
4. Click the '*Add…*' button to install the audio driver.



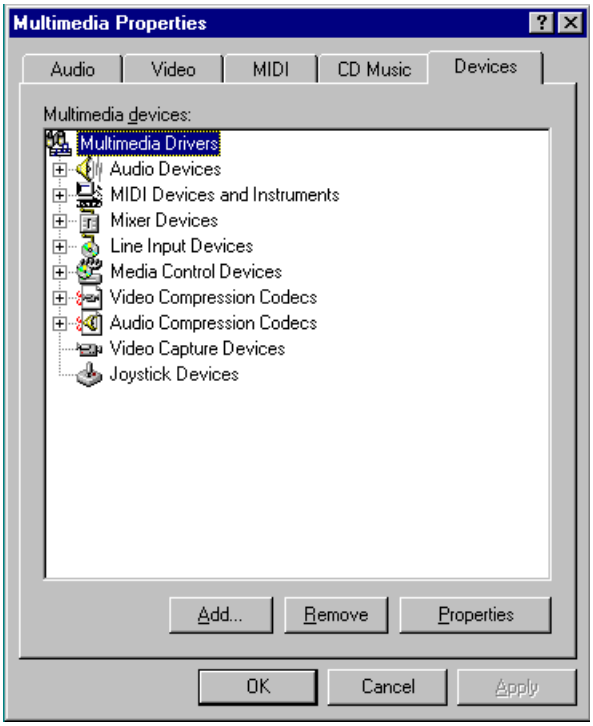
5. Select the '*VIA PCI Audio controller*' and click '*OK*' to install the audio driver.



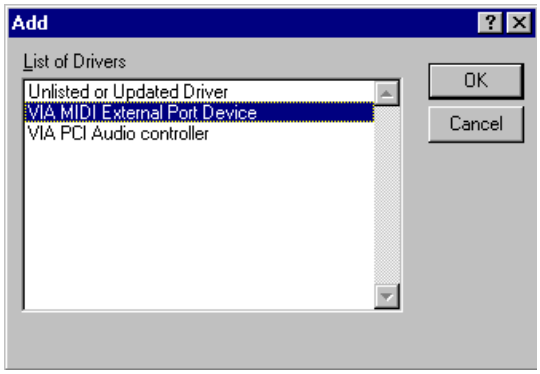
6. Click '*Don't Restart Now*' to continue the audio driver installation.



7. Click the '*Add…*' button to install the audio driver.

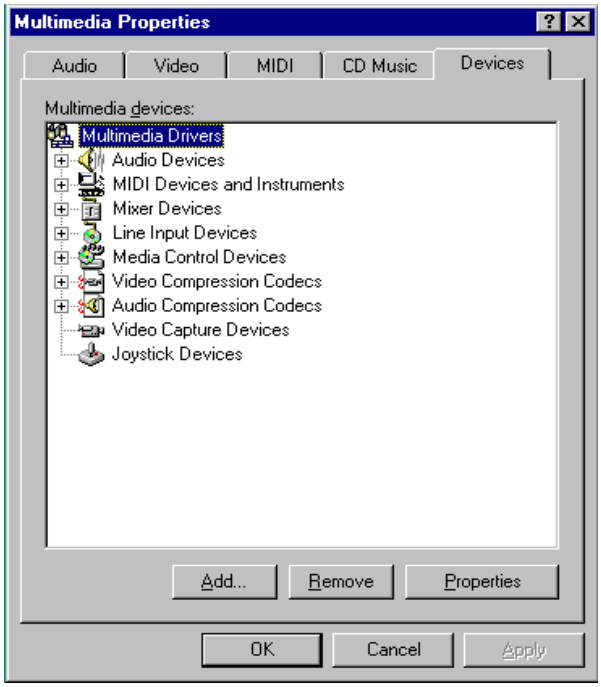


8. Select the '*VIA MIDI External Port Device*' and click '*OK*' to install the audio driver.

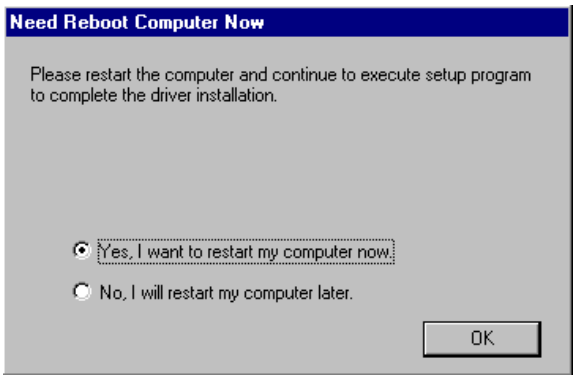


9. Click '*Don't Restart Now*' to continue the audio driver installation.

10. Click the '*OK*' button as shown below.



11. Select '*Yes, I want to restart my computer now.*' and click the '*OK*' button to complete the audio driver installation.



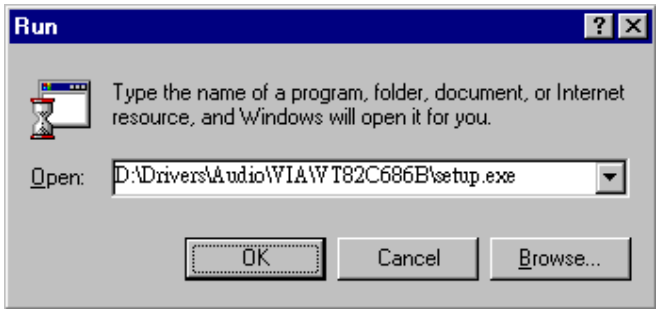
5.3.3 Windows 2000 Audio Installation

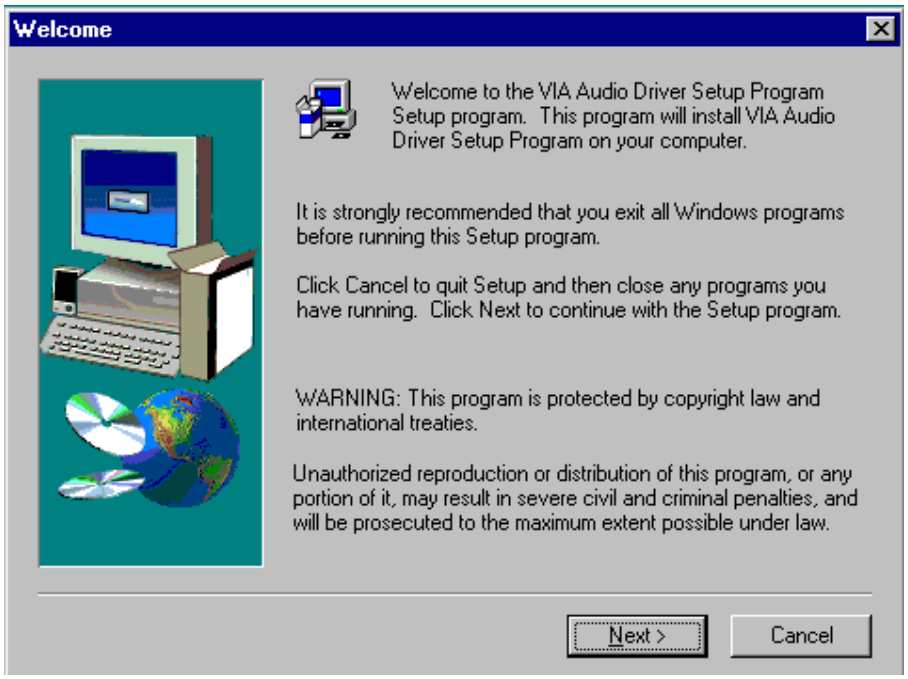
An audio driver for Windows 2000 is supplied with the system on the supporting CD-ROM.

The driver installation may be performed by the following steps:

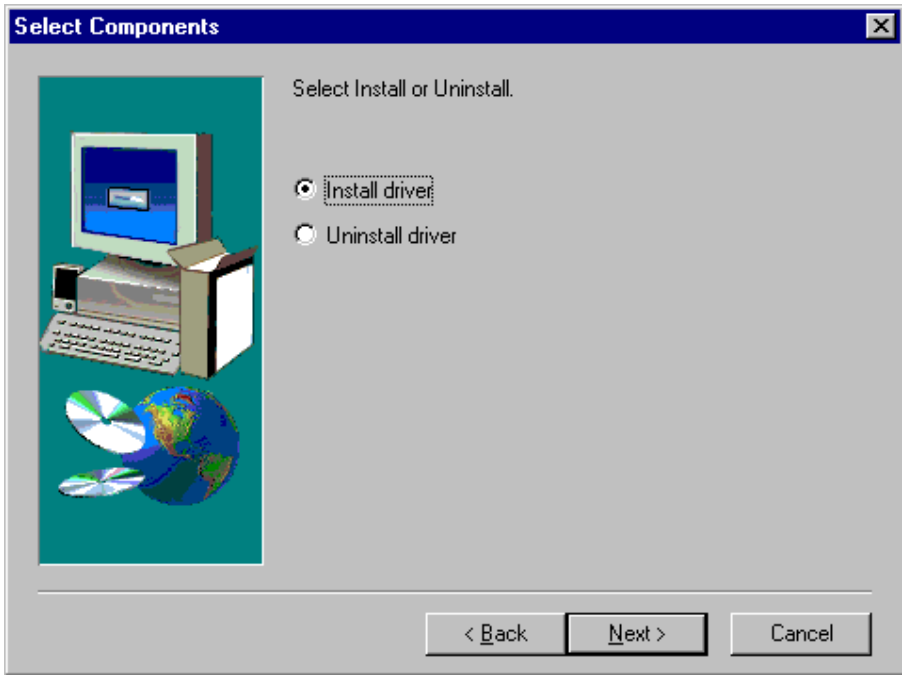
The following steps show how to install the VIA AC97 audio driver.

1. Click the '*Start*' button on the task bar, select '*Run*' and specify the location of VIA AC97 Audio driver setup program. This should start the VIA AC97 Audio driver setup program as shown below:

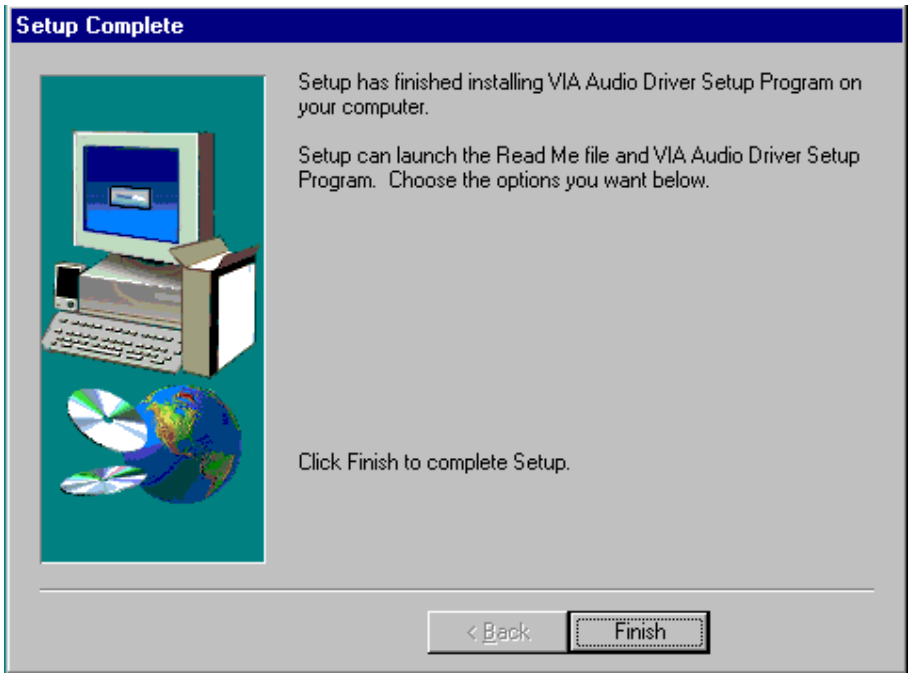




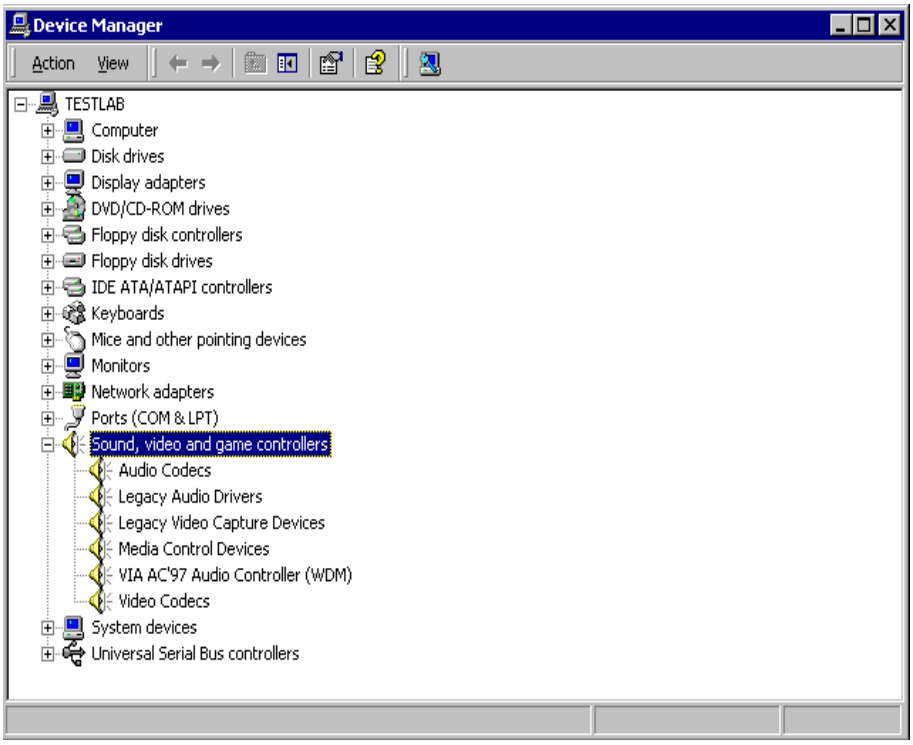
2. Select '*Install driver*' as shown below.



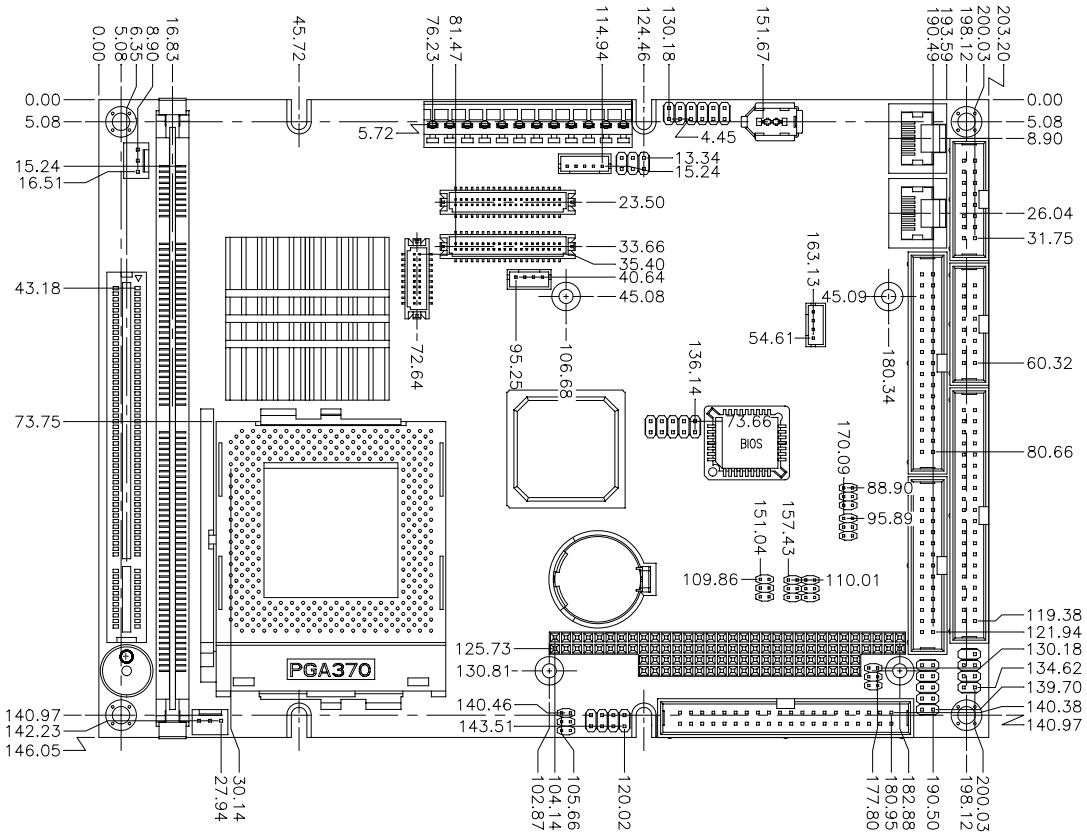
3. Click the '*Finish*' button to complete the driver setup.

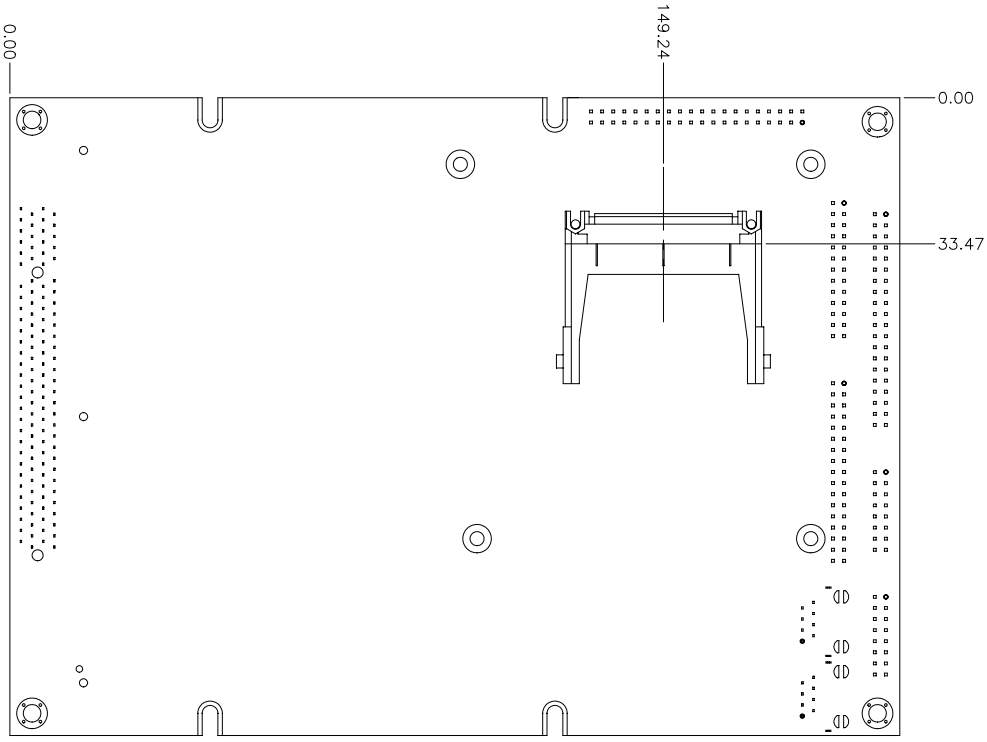


4. After running setup program, the audio driver will be automatic installed completely.
5. After the audio driver installation, the system properties will be shown as below.



6. Measurement Drawing





Appendix A: BIOS Revisions

BIOS Rev.

New Features

Bugs/Problems Solved

Known Problems

Appendix B: System Resources

Memory Map

The following table indicates memory map of EBC5612. The address ranges specify the runtime code length.

Address Range	Description	Note
00000000h-0009FFFFh	System board extension for ACPI BIOS	
000A0000h-000AFFFFh	S3 Graphics Twister	
000B0000h-000BFFFFh	S3 Graphics Twister	
000C0000h-000CDFFFh	S3 Graphics Twister	
000CE000h-000CFFFFh	System board extension for ACPI BIOS	
000F0000h-000F7FFFh	System board extension for ACPI BIOS	
000F8000h-000FBFFFh	System board extension for ACPI BIOS	
000FC000h-000FFFFFh	System board extension for ACPI BIOS	
00100000h-02FEFFFFh	System board extension for ACPI BIOS	
02FF0000h-02FFFFFFh	System board extension for ACPI BIOS	
E0000000h-E7FFFFFFh	PCI standard PCI-to-PCI bridge	
E0000000h-E7FFFFFFh	S3 Graphics Twister	
E8000000h-EBFFFFFFh	PCI standard host CPU bridge	
EC000000h-EDFFFFFFh	PCI standard PCI-to-PCI bridge	
EC000000h-EC00FFFFh	S3 Graphics Twister	
ED000000h-ED07FFFFh	S3 Graphics Twister	
EE000000h-EE0000FFh	Realtek RTL8139(A/B/C/8130) PCI Fast Ethernet (NDIS4/Win95_OSR2 driver)	
EE001000h-EE0010FFh	Realtek RTL8139(A/B/C/8130) PCI Fast Ethernet (NDIS4/Win95_OSR2 driver)	
EE002000h-EE0027FFh	PCI OHCI Compliant IEEE 1394 Host Controller	
FEE00000h-FEE00FFFh	System board extension for ACPI BIOS	
FFFF0000h-FFFFFFFFh	System board extension for ACPI BIOS	

Note:

The usage of these I/O addresses depends on the choices made in the BCM setup screen. The I/O addresses are fully usable for PC/104 interface if the corresponding on-board unit is disabled in the setup screen.

I/O – Map

The board incorporates a fully ISA Bus Compatible slave interface. The drive capabilities allow for up to four external PC/104 modules to be driven without external data buffers. The accessible I/O area on the ISA-bus is 64Kbytes with 16 address bits, whereas the accessible memory area is 16Mbytes with 24 address bits.

Certain I/O addresses are subject to change during boot as PnP managers may relocate devices or functions. The addresses shown in the table are typical locations.

I/O Port	Description	Note
0000h-000Fh	Direct memory access controller	
0010h-001Fh	Motherboard resources	
0020h-0021h	Programmable interrupt controller	
0022h-003Fh	Motherboard resources	
0040h-0043h	System timer	
0044h-005Fh	Motherboard resources	
0060h-0060h	Standard 101/102-Key or Microsoft Natural Keyboard	
0061h-0061h	System speaker	
0062h-0063h	Motherboard resources	
0064h-0064h	Standard 101/102-Key or Microsoft Natural Keyboard	
0065h-006Fh	Motherboard resources	
0070h-0073h	System CMOS/real time clock	
0074h-007Fh	Motherboard resources	
0080h-0090h	Direct memory access controller	
0091h-0093h	Motherboard resources	
0094h-009Fh	Direct memory access controller	
00A0h-00A1h	Programmable interrupt controller	
00A2h-00BFh	Motherboard resources	
00C0h-00DFh	Direct memory access controller	
00E0h-00EFh	Motherboard resources	
00F0h-00FFh	Numeric data processor	
0170h-0177h	VIA Bus Master PCI IDE Controller	
0170h-0177h	Secondary IDE controller (dual fifo)	
01F0h-01F7h	Primary IDE controller (dual fifo)	
01F0h-01F7h	VIA Bus Master PCI IDE Controller	
02E8h-02EFh	Communications Port (COM4)	
02F8h-02FFh	Communications Port (COM2)	
0376h-0376h	VIA Bus Master PCI IDE Controller	
0376h-0376h	Secondary IDE controller (dual fifo)	
0378h-037Fh	Printer Port (LPT1)	
03B0h-03BBh	S3 Graphics Twister	
03C0h-03DFh	S3 Graphics Twister	
03E8h-03EFh	Communications Port (COM3)	

I/O Port	Description	Note
03F0h-03F5h	Standard Floppy Disk Controller	
03F6h-03F6h	Primary IDE controller (dual fifo)	
03F6h-03F6h	VIA Bus Master PCI IDE Controller	
03F7h-03F7h	Standard Floppy Disk Controller	
03F8h-03FFh	Communications Port (COM1)	
04D0h-04D1h	Motherboard resources	
0CF8h-0CFFh	PCI bus	
1000h-101Fh	VIA Tech 3038 PCI to USB Universal Host Controller	
4000h-407Fh	PCI bus	
4080h-40FFh	PCI bus	
5000h-500Fh	PCI bus	
6000h-607Fh	PCI bus	
C000h-C007h	Primary IDE controller (dual fifo)	
C000h-C00Fh	VIA Bus Master PCI IDE Controller	
C008h-C00Fh	Secondary IDE controller (dual fifo)	
C400h-C41Fh	VIA Tech 3038 PCI to USB Universal Host Controller	
CC00h-CCFFh	VIA AC'97 Audio Controller (WDM)	
D000h-D003h	VIA AC'97 Audio Controller (WDM)	
D400h-D403h	VIA AC'97 Audio Controller (WDM)	
D800h-D8FFh	Realtek RTL8139(A/B/C/8130) PCI Fast Ethernet (NDIS4/Win95_OSR2 driver)	
DC00h-DCFFh	Realtek RTL8139(A/B/C/8130) PCI Fast Ethernet (NDIS4/Win95_OSR2 driver)	
E000h-E07Fh	PCI OHCI Compliant IEEE 1394 Host Controller	

Note:

The usage of these I/O addresses depends on the choices made in the BCM setup screen. The I/O addresses are fully usable for PC/104 interface if the corresponding on-board unit is disabled in the setup screen.

Interrupt Usage

The onboard VT82C686B provides an ISA compatible interrupt controller with functionality as two 8259A interrupt controllers. The two controllers are cascaded to provide 13 external interrupts. Most of them is used by onboard devices, but a few of them can be available through the PC/104 interface by disabling some onboard devices.
The actual interrupt settings depend on the PnP handler, the table below indicates the typical settings.

Interrupt	Description	Note
IRQ0	System timer	
IRQ1	Standard 101/102-Key or Microsoft Natural Keyboard	
IRQ2	Programmable interrupt controller	
IRQ3	Communications Port (COM2)	
IRQ4	Communications Port (COM1)	
IRQ5	Communications Port (COM3)	
IRQ6	Standard Floppy Disk Controller	
IRQ7	Printer Port (LPT1)	
IRQ8	System CMOS/real time clock	
IRQ9	VIA AC'97 Audio Controller (WDM)	
IRQ9	ACPI IRQ Holder for PCI IRQ Steering	
IRQ9	PCI OHCI Compliant IEEE 1394 Host Controller	
IRQ9	Realtek RTL8139(A/B/C/8130) PCI Fast Ethernet (NDIS4/Win95_OSR2 driver)	
IRQ9	VIA Tech 3038 PCI to USB Universal Host Controller	
IRQ9	ACPI IRQ Holder for PCI IRQ Steering	
IRQ9	VIA Tech 3038 PCI to USB Universal Host Controller	
IRQ10	Communications Port (COM4)	
IRQ11	Realtek RTL8139(A/B/C/8130) PCI Fast Ethernet (NDIS4/Win95_OSR2 driver)	
IRQ11	S3 Graphics Twister	
IRQ11	ACPI IRQ Holder for PCI IRQ Steering	
IRQ11	ACPI IRQ Holder for PCI IRQ Steering	
IRQ11	SCI IRQ used by ACPI bus	
IRQ12	PS/2 Compatible Mouse Port	
IRQ13	Numeric data processor	
IRQ14	Primary IDE controller (dual fifo)	
IRQ14	VIA Bus Master PCI IDE Controller	
IRQ15	VIA Bus Master PCI IDE Controller	
IRQ15	Secondary IDE controller (dual fifo)	

Note:

1. The usage of these interrupts depends on the choices made in the BCM setup screen. The interrupts are fully useable for PC/104 interface if the corresponding on-board unit is disabled in the BIOS setup.
2. These interrupt lines are managed by the PnP handler and are subject to change during system initialisation.
3. IRQ14 is routed directly from the IDE hard disk connector to the PC-AT bus. Disabling the hard disk controller in the BCM setup screen may not release the interrupt line.

DMA-channel Usage

The DMA circuitry incorporates the functionality of two 8237 DMA controllers with seven programmable channels. The controllers are referenced DMA Controller 1 for channels 0-3 and DMA Controller 2 for channels 4-7. Channel 4 is by default used to cascade the two controllers.

Channels 0-3 are hardwired to 8-bit count-by-bytes transfers and channels 5-7 to 16-bit count-by-bytes transfers.

The onboard VT82C686B provides 24-bit addressing with the 16 least significant bits [15:0] in the Current register and the most significant bits [24:16] in the Page register.

DMA-channel	Description	Note
DMA0	Available for PC/104 interface & PCI slot	
DMA1	Available for PC/104 interface & PCI slot	
DMA2	Standard Floppy Disk Controller	1
DMA3	Parallel port, if using ECP mode	1
DMA4	Used for cascading	
DMA5	Available for PC/104 interface & PCI slot	
DMA6	Available for PC/104 interface & PCI slot	
DMA7	Available for PC/104 interface & PCI slot	

Note:

The usage of these DMA-channels depends on the choices made in the BCM setup screen. The DMA-channels are fully usable for PC/104 interface if the corresponding on-board unit is disabled in the setup screen.

Appendix C: Programming the Watchdog Timer

Introduction

The EBC5612 series onboard watchdog timer is based on an 8-bit counter. The time interval is from 32 seconds to 254 minutes with a resolution of 30 seconds. As soon as the timer is out, the system will generate a reset signal.

Configure Register

The EBC5612 series onboard watchdog timer function is integrated in the I/O chip, Winbond W83977EF-AW. If you would like to utilize this function in your program, you have to know how to program the W83977EF-AW configuration register. The W83977EF-AW I/O chip decode address is 3F0h. The index port and data port is 3F1h. The way to program the register is to write the register number to index port, then read / write data from / to data port.

The following procedures show how to program the W83977EF-AW register and use the watchdog function.

1. Unlock W83977EF-AW I/O chip and enter configuration mode.
2. Select Logical Device.
3. Select register number.
4. Read / Write data from / to register.
5. Lock W83977EF-AW I/O chip and exit from configuration mode.

Programming Watchdog Timer

To Unlock / Lock W83977EF-AW and Enter / Exit configuration mode is to write a specific value to I/O Port 3F0h as shown below.

Unlock W83977EF-AW: write value 87h to I/O port 3F0h twice.
Lock W83977EF-AW: write value aah to I/O port 3F0h.
Therefore, to unlock W83977EF-AW I/O chip and enter configuration mode, write twice unlock value (87h) to port 3F0h.

```
Ex: outportb(0x3f0, 0x87);
    outportb(0x3f0, 0x87);
```

Set register 30h of logical device 8 to 1 to activate the timer.
Logical Device 8: Register number 30h (CR30)
00h: timer inactive
01h: timer active

```
Write value 7 to port 3F0h          /* register 7 (logical device switch register)*/
Write value 8 to port 3F1h          /* write value 8 to enter logical device 8 */
Ex: outportb(0x3f0, 0x07);
    outportb(0x3f1, 0x08);
```

Write time-out value (01h ~ FFh) to timer register (F2h).
Logical Device 8: Register number F2h (CRF2)
00h: Time-out Disable
01h: Time-out occurs after 32 seconds
02h: Time-out occurs after 1 minute 32 seconds
03h: Time-out occurs after 2 minutes 32 seconds
04h: Time-out occurs after 3 minutes 32 seconds
05h: Time-out occurs after 4 minutes 32 seconds

```
.
.
.
```

FFh: Time-out occurs after 254 minutes 32 seconds

Write register number F2h to port 3F0h
Write time-out value to port 3F1h

```
Ex: outportb(0x3f0, 0xF2);          /* register F2 (Watchdog Timer) */
    outportb(0x3f1, 0x01);          /* time-out value 01 = 32 seconds */
```

Lock W83977EF-AW I/O chip, and exit configuration mode
Write lock value (AAh) to port 3F0h

```
 Ex: outportb(0x3f0, 0xAA);
```

The following shows two examples of programming the watchdog timer with 32 seconds time interval in both Micro-assembly and C language.

Demo Program 1 (Micro-Assembly Language)

```
;;=============================================================
;; Title          : EBC5612 Series Watchdog Timer Demo Program (32 seconds)
;; Company        : BCM Advanced Research
;; Date           : 11/02/2000
;;=============================================================

        .model  small
        .code
W83977_IO_PORT  DW     3F0H
UNLOCK_ID    DB     087h
LOCK_ID         DB     0AAH

;;-------------------------------------------------
;; Main Program start
;;-------------------------------------------------
Watchdog PROC

;; Set Logic Device 8 Active
        mov     bl, 8                   ;; Logic Device 8
        mov     al, 30h                 ;; Register 30h
        mov     ah, 01h                 ;; Active --> 01h, InActive --> 00h
        call    W977_Register_Set

;; Set watchdog time-out value = 1  (32 seconds)
        mov     bl, 8                   ;; Logic Device 8
        mov     al, 0F2h                ;; Register F2h
        mov     ah, 01h                 ;; 01h ~ FFh  == 0:32 ~ 254:32
        call    W977_Register_Set

        mov     ah,4ch                  ;; Retuen to DOS
        int     21h
        ret
WatchDog ENDP
;;-------------------------------------------------

;;-------------------------------------------------
;; unlock W83977 register program mode
;;-------------------------------------------------
Unlock_977 proc
        cli
        push    ax
        push    dx
        mov     al, UNLOCK_ID
        mov     dx, cs:W83977_IO_PORT
        out     dx, al                  ;; write Unlock_ID to w83977 twice
        out     dx, al
```

```
        jmp     $+2
        jmp     $+2
        pop     dx
        pop     ax
        ret
Unlock_977 endp
;;-----------------------------------------------

;;-----------------------------------------------
;; lock w83977 register program mode
;;-----------------------------------------------
Lock_977 proc
        push    ax
        push    dx
        mov     dx, cs:W83977_IO_PORT
        mov     al, LOCK_ID
        out     dx, al
        pop     dx
        pop     ax
        ret
Lock_977 endp
;;-----------------------------------------------

;;-----------------------------------------------
;; Select W83977 I/O chip Logic Device
;; bl : Device Number
;;-----------------------------------------------
Set_Device proc
        push    ax
        push    dx
        mov     dx, cs:W83977_IO_PORT
        mov     al, 07h
        out     dx, al
        inc     dx
        mov     al, bl
        out     dx, al
        pop     dx
        pop     ax
        ret
Set_Device endp
```

```
;;-------------------------------------------------

;;-------------------------------------------------
;; Write data to W83977 Register
;;  al : register number
;;  ah : data
;;  bl : device number
;;-------------------------------------------------
W977_Register_Set PROC
        push    dx
        call      Unlock_977
        call      Set_Device
        mov     dx, cs: W83977_IO_PORT
        out       dx, al
        mov     al, ah
        inc      dx
        out      dx, al
        call     Lock_977
        pop     dx
        ret
W977_Register_Set ENDP
;;-------------------------------------------------

        end
```

Demo Program 2 (C Language)

```
//=============================================================
//  Title        : EBC5612 Series Watchdog Timer Test Utility
// Company  : BCM Advanced Research
// Programer: Winston Kang
// Version     : 1.0
// Date        : 11/02/2000
// Compiler   : Borland C ++
//=============================================================

#include <stdio.h>
#include <stdlib.h>
#include <conio.h>

#define IO_INDEX_PORT       0x3F0
#define IO_DATA_PORT        0x3F1
#define UNLOCK_DATA         0x87
#define LOCK_DATA           0xAA
#define DEVICE_REGISTER  0x07

void EnterConfigMode()
{
   outportb(IO_INDEX_PORT, UNLOCK_DATA);
   outportb(IO_INDEX_PORT, UNLOCK_DATA);
}

void ExitConfigMode()
{
   outportb(IO_INDEX_PORT, LOCK_DATA);
}

void SelectDevice(unsigned char device)
{
   outportb(IO_INDEX_PORT, DEVICE_REGISTER);
   outportb(IO_DATA_PORT, device);
}

unsigned char ReadAData(short int reg)
{
   outportb(IO_INDEX_PORT, reg);
   return (inportb(IO_DATA_PORT));
}

void WriteAData(unsigned char reg, unsigned char data)
{
   outportb(IO_INDEX_PORT, reg);
   outportb(IO_DATA_PORT, data);
}
```

```
void SetWatchDogTime(unsigned char time_val)
{
   EnterConfigMode();
   SelectDevice(8);
      //Set Register F2
               //Set Watch-Dog Timer
   WriteAData(0xF2, time_val);
               //Set Register 30
               //Set Device 8 Function enable
   WriteAData(0x30, 0x01);
   ExitConfigMode();
}
int Detect_W83977EF()
{
   EnterConfigMode();
   if (ReadAData(0x20) == 0x52 && ReadAData(0x21) == 0xF4)
               return 0;
   else
               return 1;
}
void main(int argc, char* argv[])
{
  int time_value=0;
  char *ptr;
  printf("WinBond 83977EF WatchDog Timer Test Utility Version 1.0 \n");
  printf("Copyright (c) 2000 BCM Advanced Research\n");
  printf("(only support EBC5612 board and will reset the system)\n");
  if (argc == 1)
   {  printf("\n Syntax: 5610WDT  [step] \n");
      printf(" step range : 1 ~ 256 steps \n");
      printf(" timer range: 0:32 ~ 254:32 (min:sec) \n");
      return ;
    }
  if (Detect_W83977EF()==1)
   {  printf("Sorry ! Can't found W83977EF I/O Chip!");
      return ;
   }
  if (argc > 1)
   {
      ptr = argv[1];
      time_value = atoi(ptr);
   }
  if (time_value > 0 && time_value < 256)
   {
      SetWatchDogTime((unsigned char) time_value);
      printf("Watch Dog reset Timer set up : %02d:%02d ",(time_value-1),
                                                32);
   }
}
```

Appendix D: AWARD BIOS POST Messages

During the Power on Self-Test (POST), if the BIOS detects an error requiring you to do something to fix, it will either sound a beep code or display a message.

If a message is displayed, it will be accompanied by:

PRESS F1 TO CONTINUE, CTRL-ALT-ESC OR DEL TO ENTER SETUP

POST Beep

Currently there are two kinds of beep codes in BIOS. This code indicates that a video error has occurred and the BIOS cannot initialize the video screen to display any additional information. This beep code consists of a single long beep followed by two short beeps. The other code indicates that your DRAM error has occurred. This beep code consists of a single long beep repeatedly.

Error Messages

One or more of the following messages may be displayed if the BIOS detect an error during the POST. This list includes messages for both the ISA and the EISA BIOS.

CMOS BATTERY HAS FAILED

CMOS battery is no longer functional. It should be replaced.

CMOS CHECKSUM ERROR

Checksum of CMOS is incorrect. This can indicate that CMOS has become corrupt. This error may have been caused by a weak battery. Check the battery and replace if necessary.

DISK BOOT FAILURE, INSERT SYSTEM DISK AND PRESS ENTER

No boot device was found. This could mean that either a boot drive was not detected or the drive does not contain proper system boot files. Insert a system disk into Drive A: and press <Enter>. If you assumed the system would boot from the hard drive, make sure the controller is inserted correctly and all cables are properly attached. Also be sure the disk is formatted as a boot device. Then reboot the system.

DISKETTE DRIVES OR TYPES MISMATCH ERROR - RUN SETUP

Type of diskette drive installed in the system is different from the CMOS definition. Run Setup to reconfigure the drive type correctly.

DISPLAY SWITCH IS SET INCORRECTLY

Display switch on the motherboard can be set to either monochrome or color. This indicates the switch is set to a different setting than indicated in Setup. Determine which setting is correct, and then either turn off the system and change the jumper, or enter Setup and change the VIDEO selection.

DISPLAY TYPE HAS CHANGED SINCE LAST BOOT

Since last powering off the system, the display adapter has been changed. You must configure the system for the new display type.

EISA Configuration Checksum Error
PLEASE RUN EISA CONFIGURATION UTILITY

The EISA non-volatile RAM checksum is incorrect or cannot correctly read the EISA slot. This can indicate either the EISA non-volatile memory has become corrupt or the slot has been configured incorrectly. Also be sure the card is installed firmly in the slot.

EISA Configuration Is Not Complete
PLEASE RUN EISA CONFIGURATION UTILITY

The slot configuration information stored in the EISA non-volatile memory is incomplete.

Note: When either of these errors appear, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

ERROR ENCOUNTERED INITIALIZING HARD DRIVE

Hard drive cannot be initialized. Be sure the adapter is installed correctly and all cables are correctly and firmly attached. Also be sure the correct hard drive type is selected in Setup.

ERROR INITIALIZING HARD DISK CONTROLLER

Cannot initialize controller. Make sure the cord is correctly and firmly installed in the bus. Be sure the correct hard drive type is selected in Setup. Also check to see if any jumper needs to be set correctly on the hard drive.

FLOPPY DISK CNTRLR ERROR OR NO CNTRLR PRESENT

Cannot find or initialize the floppy drive controller. Make sure the controller is installed correctly and firmly. If there are no floppy drives installed, be sure the Diskette Drive selection in Setup is set to NONE.

Invalid EISA Configuration
PLEASE RUN EISA CONFIGURATION UTILITY

The non-volatile memory containing EISA configuration information was programmed incorrectly or has become corrupt. Re-run EISA configuration utility to correctly program the memory.

NOTE: When this error appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

KEYBOARD ERROR OR NO KEYBOARD PRESENT

Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during the boot.

If you are purposely configuring the system without a keyboard, set the error halt condition in Setup to HALT ON ALL, BUT KEYBOARD. This will cause the BIOS to ignore the missing keyboard and continue the boot.

Memory Address Error at ...

Indicates a memory address error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory chips.

Memory parity Error at ...

Indicates a memory parity error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory chips.

MEMORY SIZE HAS CHANGED SINCE LAST BOOT

Memory has been added or removed since the last boot. In EISA mode use Configuration Utility to reconfigure the memory configuration. In ISA mode enter Setup and enter the new memory size in the memory fields.

Memory Verify Error at ...

Indicates an error verifying a value already written to memory. Use the location along with your system's memory map to locate the bad chip.

OFFENDING ADDRESS NOT FOUND

This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem cannot be isolated.

OFFENDING SEGMENT:

This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem has been isolated.

PRESS A KEY TO REBOOT

This will be displayed at the bottom screen when an error occurs that requires you to reboot. Press any key and the system will reboot.

PRESS F1 TO DISABLE NMI, F2 TO REBOOT

When BIOS detects a Non-maskable Interrupt condition during boot, this will allow you to disable the NMI and continue to boot, or you can reboot the system with the NMI enabled.

RAM PARITY ERROR - CHECKING FOR SEGMENT...

Indicates a parity error in Random Access Memory.

Should Be Empty But EISA Board Found
PLEASE RUN EISA CONFIGURATION UTILITY

A valid board ID was found in a slot that was configured as having no board ID.

NOTE; When this error appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

Should Have EISA Board But Not Found
PLEASE RUN EISA CONFIGURATION UTILITY

The board installed is not responding to the ID request, or no board ID has been found in the indicated slot.

NOTE: When this error appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

Slot Not Empty

Indicates that a slot designated as empty by the EISA Configuration Utility actually contains a board.

NOTE: When this error appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

SYSTEM HALTED, (CTRL-ALT-DEL) TO REBOOT...

Indicates the present boot attempt has been aborted and the system must be rebooted. Press and hold down the CTRL and ALT keys and press DEL.

Wrong Board In Slot
PLEASE RUN EISA CONFIGURATION UTILITY

The board ID does not match the ID stored in the EISA non-volatile memory.

NOTE: When this error appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

Floppy DISK(S) fail (80) → Unable to reset floppy subsystem.

FLOPPY DISK(S) fail (40) → Floppy Type dismatch.

Hard Disk(s) fail (80) → HDD reset failed

Hard Disk(s) fail (40) → HDD controller diagnostics failed.

Hard Disk(s) fail (20) → HDD initialization error.

Hard Disk(s) fail (10) → Unable to recalibrate fixed disk.

Hard Disk(s) fail (08) → Sector Verify failed.

Keyboard is locked out - Unlock the key.
BIOS detect the keyboard is locked. P17 of keyboard controller is pulled low.

Keyboard Error or no keyboard present.
Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during the boot.

Manufacturing POST Loop.
System will repeat POST procedure infinitely while the P15 of keyboard controller is pull low. This is also used for M/B burn in test.

BIOS ROM Checksum error - System halted.
The checksum of ROM address F0000H-FFFFFH is bad.

Memory Test Fail.
BIOS reports the memory test fail if the onboard memory is tested error.

Appendix E: AWARD BIOS POST Codes

POST (hex)	Description
CFh	Test CMOS R/W functionality.
C0h	Early chipset initialization: -Disable shadow RAM -Disable L2 cache (socket 7 or below) -Program basic chipset registers
C1h	Detect memory -Auto-detection of DRAM size, type and ECC. -Auto-detection of L2 cache (socket 7 or below)
C3h	Expand compressed BIOS code to DRAM
C5h	Call chipset hook to copy BIOS back to E000 & F000 shadow RAM.
0h1	Expand the Xgroup codes locating in physical address 1000:0
02h	Reserved
03h	Initial Superio_Early_Init switch.
04h	Reserved
05h	1. Blank out screen 2. Clear CMOS error flag
06h	Reserved
07h	1. Clear 8042 interface 2. Initialize 8042 self-test
08h	1. Test special keyboard controller for Winbond 977 series Super I/O chips. 2. Enable keyboard interface.
09h	Reserved
0Ah	1. Disable PS/2 mouse interface (optional). 2. Auto detect ports for keyboard & mouse followed by a port & interface swap (optional). 3. Reset keyboard for Winbond 977 series Super I/O chips.
0Bh	Reserved
0Ch	Reserved
0Dh	Reserved
0Eh	Test F000h segment shadow to see whether it is R/W-able or not. If test fails, keep beeping the speaker.
0Fh	Reserved
10h	Auto detect flash type to load appropriate flash R/W codes into the run time area in F000 for ESCD & DMI support.
11h	Reserved
12h	Use walking 1's algorithm to check out interface in CMOS circuitry. Also set real-time clock power status, and then check for override.

POST (hex)	Description
13h	Reserved
14h	Program chipset default values into chipset. Chipset default values are MODBINable by OEM customers.
15h	Reserved
16h	Initial Early_Init_Onboard_Generator switch.
17h	Reserved
18h	Detect CPU information including brand, SMI type (Cyrix or Intel) and CPU level (586 or 686).
19h	Reserved
1Ah	Reserved
1Bh	Initial interrupts vector table. If no special specified, all H/W interrupts are directed to SPURIOUS_INT_HDLR & S/W interrupts to SPURIOUS_soft_HDLR.
1Ch	Reserved
1Dh	Initial EARLY_PM_INIT switch.
1Eh	Reserved
1Fh	Load keyboard matrix (notebook platform)
20h	Reserved
21h	HPM initialization (notebook platform)
22h	Reserved
23h	1. Check validity of RTC value: e.g. a value of 5Ah is an invalid value for RTC minute. 2. Load CMOS settings into BIOS stack. If CMOS checksum fails, use default value instead. 3. Prepare BIOS resource map for PCI & PnP use. If ESCD is valid, take into consideration of the ESCD's legacy information. 4. Onboard clock generator initialization. Disable respective clock resource to empty PCI & DIMM slots. 5. Early PCI initialization: -Enumerate PCI bus number -Assign memory & I/O resource -Search for a valid VGA device & VGA BIOS, and put it into C000:0.
24h	Reserved
25h	Reserved
26h	Reserved
27h	Initialize INT 09 buffer
28h	Reserved
29h	1. Program CPU internal MTRR (P6 & PII) for 0-640K memory address. 2. Initialize the APIC for Pentium class CPU. 3. Program early chipset according to CMOS setup. Example: onboard IDE controller. 4. Measure CPU speed. 5. Invoke video BIOS.

POST (hex)	Description
2Ah	Reserved
2Bh	Reserved
2Ch	Reserved
2Dh	1. Initialize multi-language 2. Put information on screen display, including Award title, CPU type, CPU speed ….
2Eh	Reserved
2Fh	Reserved
30h	Reserved
31h	Reserved
32h	Reserved
33h	Reset keyboard except Winbond 977 series Super I/O chips.
34h	Reserved
35h	Reserved
36h	Reserved
37h	Reserved
38h	Reserved
39h	Reserved
3Ah	Reserved
3Bh	Reserved
3Ch	Test 8254
3Dh	Reserved
3Eh	Test 8259 interrupt mask bits for channel 1.
3Fh	Reserved
40h	Test 8259 interrupt mask bits for channel 2.
41h	Reserved
42h	Reserved
43h	Test 8259 functionality.
44h	Reserved
45h	Reserved
46h	Reserved
47h	Initialize EISA slot
48h	Reserved
49h	1. Calculate total memory by testing the last double word of each 64K page. 2. Program writes allocation for AMD K5 CPU.
4Ah	Reserved
4Bh	Reserved
4Ch	Reserved
4Dh	Reserved

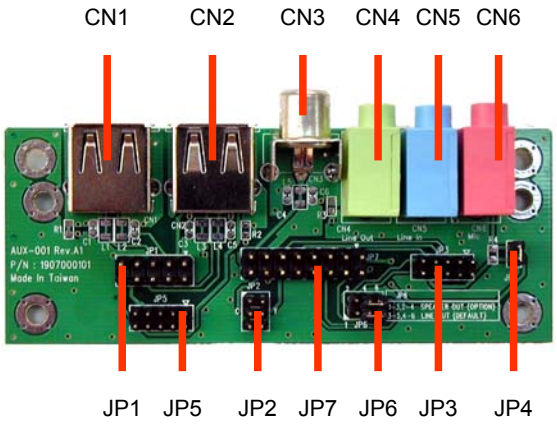
POST (hex)	Description
4Eh	1. Program MTRR of M1 CPU 2. Initialize L2 cache for P6 class CPU & program CPU with proper cacheable range. 3. Initialize the APIC for P6 class CPU. 4. On MP platform, adjust the cacheable range to smaller one in case the cacheable ranges between each CPU are not identical.
4Fh	Reserved
50h	Initialize USB
51h	Reserved
52h	Test all memory (clear all extended memory to 0)
53h	Reserved
54h	Reserved
55h	Display number of processors (multi-processor platform)
56h	Reserved
57h	1. Display PnP logo 2. Early ISA PnP initialization -Assign CSN to every ISA PnP device.
58h	Reserved
59h	Initialize the combined Trend Anti-Virus code.
5Ah	Reserved
5Bh	(Optional Feature) Show message for entering AWDFLASH.EXE from FDD (optional)
5Ch	Reserved
5Dh	1. Initialize Init_Onboard_Super_IO switch. 2. Initialize Init_Onbaord_AUDIO switch.
5Eh	Reserved
5Fh	Reserved
60h	Okay to enter Setup utility; i.e. not until this POST stage can users enter the CMOS setup utility.
61h	Reserved
62h	Reserved
63h	Reserved
64h	Reserved
65h	Initialize PS/2 Mouse
66h	Reserved
67h	Prepare memory size information for function call: INT 15h ax=E820h
68h	Reserved
69h	Turn on L2 cache
6Ah	Reserved
6Bh	Program chipset registers according to items described in Setup & Auto-configuration table.

POST (hex)	Description
6Ch	Reserved
6Dh	1. Assign resources to all ISA PnP devices. 2. Auto assign ports to onboard COM ports if the corresponding item in Setup is set to “AUTO”.
6Eh	Reserved
6Fh	1. Initialize floppy controller 2. Set up floppy related fields in 40:hardware.
70h	Reserved
71h	Reserved
72h	Reserved
73h	(Optional Feature) Enter AWDFLASH.EXE if : -AWDFLASH is found in floppy drive. -ALT+F2 is pressed
74h	Reserved
75h	Detect & install all IDE devices: HDD, LS120, ZIP, CDROM…..
76h	Reserved
77h	Detect serial ports & parallel ports.
78h	Reserved
79h	Reserved
7Ah	Detect & install co-processor
7Bh	Reserved
7Ch	Reserved
7Dh	Reserved
7Eh	Reserved
7Fh	1. Switch back to text mode if full screen logo is supported. -If errors occur, report errors & wait for keys -If no errors occur or F1 key is pressed to continue: ◆Clear EPA or customization logo.
80h	Reserved
81h	Reserved
82h	1. Call chipset power management hook. 2. Recover the text fond used by EPA logo (not for full screen logo) 3. If password is set, ask for password.
83h	Save all data in stack back to CMOS
84h	Initialize ISA PnP boot devices
85h	1. USB final Initialization 2. NET PC: Build SYSID structure 3. Switch screen back to text mode 4. Set up ACPI table at top of memory. 5. Invoke ISA adapter ROMs 6. Assign IRQs to PCI devices 7. Initialize APM 8. Clear noise of IRQs.

POST (hex)	Description
86h	Reserved
87h	Reserved
88h	Reserved
89h	Reserved
90h	Reserved
91h	Reserved
92h	Reserved
93h	Read HDD boot sector information for Trend Anti-Virus code
94h	1. Enable L2 cache 2. Program boot up speed 3. Chipset final initialization. 4. Power management final initialization 5. Clear screen & display summary table 6. Program K6 write allocation 7. Program P6 class write combining
95h	1. Program daylight saving 2. Update keyboard LED & typematic rate
96h	1. Build MP table 2. Build & update ESCD 3. Set CMOS century to 20h or 19h 4. Load CMOS time into DOS timer tick 5. Build MSIRQ routing table.
FFh	Boot attempt (INT 19h)

Appendix F: Audio / USB Daughter Board User's Guide

Jumper & Connector Layout



Jumper & Connector List

Jumpers		
Label	**Function**	**Note**
JP1	2.54mm pitch USB connector for Mini module series	5 x 2 header, pitch 2.54mm
JP2	Reserve for S-terminal testing	3 x 2 header, pitch 2.0mm
JP3	Audio connector for Micro module series	5 x 2 header, pitch 2.0mm
JP4	Reserved	
JP5	2.00mm pitch USB connector for Micro module series	5 x 2 header, pitch 2.0mm
JP6	Line out / Speaker out select	1-3, 2-4 Speaker out 3-5, 4-6 Line out (Default)
JP7	TV / Audio connector for Mini module series	8 x 2 header, pitch 2.54mm

Connectors		
Label	**Function**	**Note**
CN1	USB 1 connector	
CN2	USB 2 connector	
CN3	TV output RCA jack	
CN4	Line out or Speaker out	Select by JP6
CN5	Line in	
CN6	Mic in	

Measurement Drawing