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KONTRON KTG41/ATXU USER MANUAL



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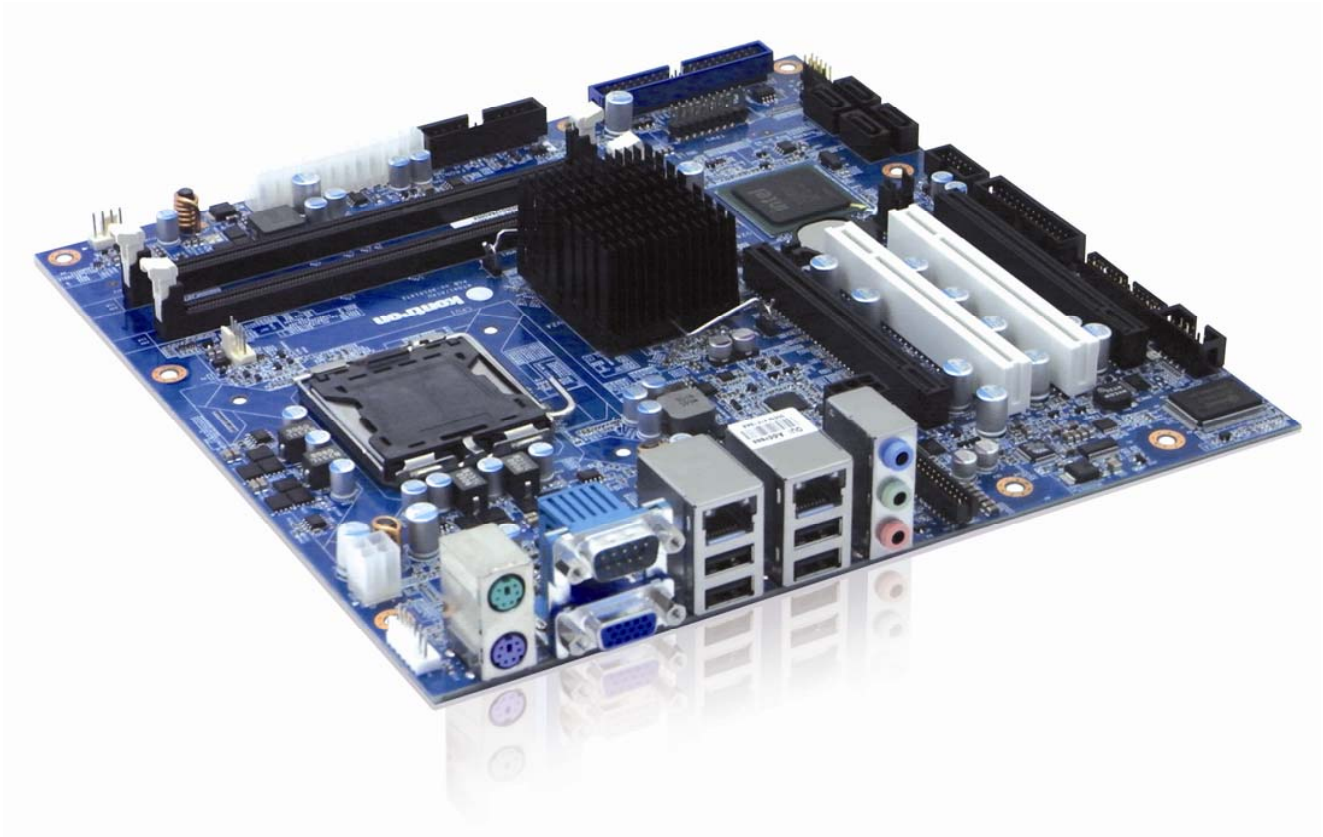
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KTG41/ATXu

KTG41 Users Guide

KTD-00781-A

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Document revision history.

Revision	Date	By	Comment
A	Nov. 16th 2009	MLA	Added “mounting the board to chassis”. Correction of RAM PN.
0	Sep. 24th 2009	JSE/MLA	Initial release

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- CPU Board
  1. Type.
  2. Part Number (find PN on label)
  3. Serial Number if available (find SN on label)
- Configuration
  1. CPU Type, Clock speed
  2. DRAM Type and Size.
  3. BIOS Revision (Find the Version Info in the BIOS Setup).
  4. BIOS Settings different than *Default* Settings (Refer to the BIOS Setup Section).
- System
  1. O/S Make and Version.
  2. Driver Version numbers (Graphics, Network, and Audio).
  3. Attached Hardware: Harddisks, CD-rom, LCD Panels etc.

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Introduction

This manual describes the KTG41/ATXu board made by KONTRON Technology A/S. The board will also be denoted KTG41.

The KTQ41 boards supports the Intel® Core™2 Quad processor Q9000 series, the Intel® Core™2 Duo processor E7000 and E8000 series with a maximum TDP of 95W. These processors belong to the Intel Yorkfield and Wolfdale families.

Use of this Users Guide implies a basic knowledge of PC-AT hard- and software. This manual is focused on describing the KTG41 special features and is not intended to be a standard PC-AT textbook.

New users are recommended to study the short installation procedure stated in the following chapter before switching-on the power.

All configuration and setup of the CPU board is either done automatically or by the user in the CMOS setup menus, except for the CMOS Clear jumper (JBAT1), SPI jumper (JP6), Interface BIOS jumper (JP4 and JP5).

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1 Installation procedure

1.1 Installing the board

To get the board running, follow these steps. In some cases the board shipped from KONTRON Technology has DDR3 DRAM mounted. In this case Step 2 can be skipped.

1. **Turn off the power supply**

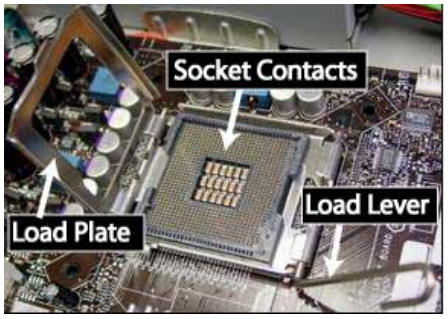
Warning: Do not use Power Supply without 3.3V monitoring watchdog, which is standard feature in ATX Power Supplies.
Running the board without 3.3V connected will damage the board after a few minutes.

2. **Insert the DDR3 DIMM 240pin DRAM module(s)**
Be careful to push it in the slot(s) before locking the tabs. For a list of approved DDR3 DIMM modules contact your Distributor or FAE.
DDR3-800/1066 DIMM 240pin DRAM modules (PC3-6400/PC3-8500) are supported.



DDR3 Memory DIMM:
Socket 1
Socket 2

3. **Install the processor**
The CPU is keyed and will only mount in the CPU socket in one way. Use the handle to open/ close the CPU socket. The Intel® Core™2 Quad, Intel® Core™2 Duo in the LGA775 package are supported, refer to supported processor overview for details.





Do NOT touch socket contacts

Opening the socket:
Apply pressure to the corner with right hand thumb while opening/closing the load lever, otherwise lever can bounce back like a “mouse trap” and WILL cause bent contacts (when loaded)

1. Disengage Load Lever by depressing down and out on the hook to clear retention tab
2. Rotate Load Lever to fully open position at approximately 135°
3. Rotate Load Plate to fully open position at approximately 100°

Remove Socket Protective Cover
With left hand index finger and thumb to support the load plate edge, engage protective cover finger tab with right hand thumb and peel the cover from LGA775 Socket while pressing on center of protective cover to assist in removal.
Set protective cover aside. Always put cover back on if the processor is removed from the socket.

IMPORTANT:
For return goods (RMA): warranty is void if board is returned without Protective cover.

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Visually inspect protective cover for damage
If damage observed, replace the cover.
Note: After cover removal, make sure socket load plate and contacts are free of foreign material. Debris may be removed with compressed air.
Note: Removing protective cover after CPU insertion will compromise the ability to visually inspect socket.

Processor Installation
Locate Connection 1 indicator and the two orientation key notches.
Grasp the processor with thumb and index finger. (Grasp the edges without the orientation notches.) The socket has cutouts for your fingers to fit into.
Carefully place the package into the socket body using a purely vertical motion. (Tilting the processor into place or shifting it into place on the socket can damage the sensitive socket contacts.)
CAUTION: Recommend not to use a Vacuum Pen for installation.
Verify that package is within the socket body and properly mated to the orientation keys
Close the socket by:

A. Close the Load Plate
B. While pressing down lightly on Load Plate, engage the Load Lever.
C. Secure Load Lever with Load Plate tab under retention tab of Load Lever

4. **Cooler Installation**
   Use heat paste or adhesive pads between CPU and cooler and connect the Fan electrically to the FAN_CPU connector.

5. **Connecting Interfaces**
   Insert all external cables for hard disk, keyboard etc. A CRT monitor must be connected in order to change CMOS settings. When using bootable SATA disk, then connect to SATA0 or SATA2 or select in BIOS “ATA/IDE Configuration” = Enhanced.

6. **Connect Power supply**
   Connect power supply to the board by the ATX/ BTXPWR and 4-pin ATX connectors. For board to operate connection of both the ATX/BTX and 4-pin ATX (12V) connectors are required.

7. **Turn on the power on the ATX/ BTX power supply**

8. **Power Button**
   The PWRBTN_IN must be toggled to start the Power supply; this is done by shorting pins 16 (PWRBTN_IN) and pin 18 (GND) on the FRONTPNL connector (see Connector description). A “normally open” switch can be connected via the FRONTPNL connector.

9. **BIOS Setup**
   Enter the BIOS setup by pressing the <Del> key during boot up.
   Enter Exit Menu and Load Optimal Defaults.
   Refer to the “BIOS Configuration / Setup“ section of this manual for details on BIOS setup.

Note: To clear all CMOS settings, including Password protection, move the Clr-CMOS jumper (with or without power) for approximately 1 minute. This will also disable any Secure CMOS setup on the board. Alternatively, turn off power and remove the battery for 1 minute, but be careful to orientate the battery correctly when reinserted.

10. **Mounting the board to chassis**



Warning: When mounting the board to chassis etc. please notice that the board contains components on both sides of the PCB which can easily be damaged if board is handled without reasonable care. A damaged component can result in malfunction or no function at all.

When fixing the Motherboard on a chassis it is recommended using screws with integrated washer and having diameter of ~7mm.
Note: Do not use washers with teeth, as they can damage the PCB mounting hole and may cause short circuits.

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1.2 Requirement according to EN60950

Users of KTG41 should take care when designing chassis interface connectors in order to fulfil the EN60950 standard:

When an interface/connector has a VCC (or other power) pin, which is directly connected to a power plane like the VCC plane:

To protect the external power lines of the peripheral devices, the customer has to take care about:

- That the wires have suitable rating to withstand the maximum available power.
- That the enclosure of the peripheral device fulfils the fire protecting requirements of IEC/EN 60950.

Lithium Battery precautions:

CAUTION! Danger of explosion if battery is incorrectly replaced. Replace only with same or equivalent type recommended by manufacturer. Dispose of used batteries according to the manufacturer's instructions.	**VORSICHT!** Explosionsgefahr bei unsachgemäßem Austausch der Batterie. Ersatz nur durch den selben oder einen vom Hersteller empfohlenen gleichwertigen Typ. Entsorgung gebrauchter Batterien nach Angaben des Herstellers.
ADVARSEL! Lithiumbatteri – Eksplosionsfare ved fejlagtig håndtering. Udskiftning må kun ske med batteri af samme fabrikat og type. Levér det brugte batteri tilbage til leverandøren.	**ADVARSEL** Eksplosjonsfare ved feilaktig skifte av batteri. Benytt samme batteritype eller en tilsvarende type anbefalt av apparatfabrikanten. Brukte batterier kasseres i henhold til fabrikantens instruksjoner.
VARNING Explosionsfara vid felaktigt batteribyte. Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren. Kassera använt batteri enligt fabrikantens instruktion.	**VAROITUS** Paristo voi räjähtää, jos se on virheellisesti asennettu. Vaihda paristo ainoastaan laltevalmistajan suosittelemaan tyyppiln. Hävitä käytetty paristo valmistajan ohjeiden mukaisesti.

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2 System specification

2.1 Component main data

The table below summarizes the features of the KTG41/ATXu embedded motherboard.

Form factor	KTG41/ATXu: Micro-ATX (243,84millimeters by 243,84millimeters)
Processor	• Support for Supports Intel® Core™2 Quad processor Q9000 series, Supports Intel® Core™2 Duo processor E7000 and E8000 in LGA775 package with up to 1333MHz system bus and 3/6/12MB internal cache. • Support for Yorkfield (45 nanometre) and Wolfdale (45 nanometre) family processors.
Memory	• 2 pcs. DDR3 DIMM 240pin DRAM sockets. • Support for DDR 800/1066MHz (PC3-6400/PC3-8500) • Support system memory from 512MB and up to 4GB (*). (*) Less than 4GB displayed in System Properties using 32bit OS. (Shared Video Memory/PCI resources are withdrawn). • ECC not supported
Chipset	Intel G41 Chipset consisting of: • Intel® AC82G41 Graphics Memory Controller Hub (GMCH) • Intel® ICH7R I/O Controller Hub (ICH7R)
Video	• Intel® GMA X4500 graphics engine • Dynamic Video Memory Technology (DVMT 5.0), allowing up to 384MB dynamically allocated Video Memory (System memory is allocated when it is needed). • Analogue Display Support CRT, 350-MHz, 24 bit integrated RAMDAC with support for analogue monitors up to 2048 x 1536 @ 75 Hz • Native Display port and DVI support. The digital ports are multiplexed on to the PEG interface using passive PEG card (Accessory). • Serial Digital Video Out (SDVO) ports (2 channels) for additional CRT, LVDS panel, DVI, TV-Out and/or HDMI support via Advanced Digital Display 2 (ADD2) cards or Media Expansion Cards. • Dual independent pipe support, Mirror and Dual independent display support • Dual Monitor support with combinations of SDVO port devices and onboard CRT
Audio	Audio, 7.1 and 7.2 Channel High Definition Audio Codec using the VIA 1708B codec • Line-out • Line-in • Surround output: SIDE, LFE, CEN, BACK and FRONT • Microphone: MIC1 • CDROM in • SPDIF Interface • Onboard speaker
I/O Control	Winbond W83627DHG LPC Bus I/O Controller
Peripheral interfaces	• Four USB 2.0 ports on I/O area • Four USB 2.0 ports on internal pinrows • Two Serial ports (RS232) • One Parallel port, SPP/EPP/ECP • Four Serial ATA-300 IDE interfaces with RAID 0/1/5/10 support • One Ultra PATA 100/66/33 IDE interface supporting two drives • PS/2 keyboard and mouse ports
LAN Support	• 2x 10/100/1000Mbits/s LAN using Marvell 88E8071 controllers • RPL/PXE netboot supported. Wake On LAN (WOL) supported.
BIOS	• Kontron Technology / AMI BIOS (core version) • Support for Advanced Configuration and Power Interface (ACPI 3.0), Plug and Play ○ Suspend To Ram ○ Suspend To Disk ○ Intel Speed Step • Secure CMOS/ OEM Setup Defaults • “Always On” BIOS power setting • RAID Support (RAID modes 0, 1, 5 and 10) (for Linux O/S only RAID 0 and 1)

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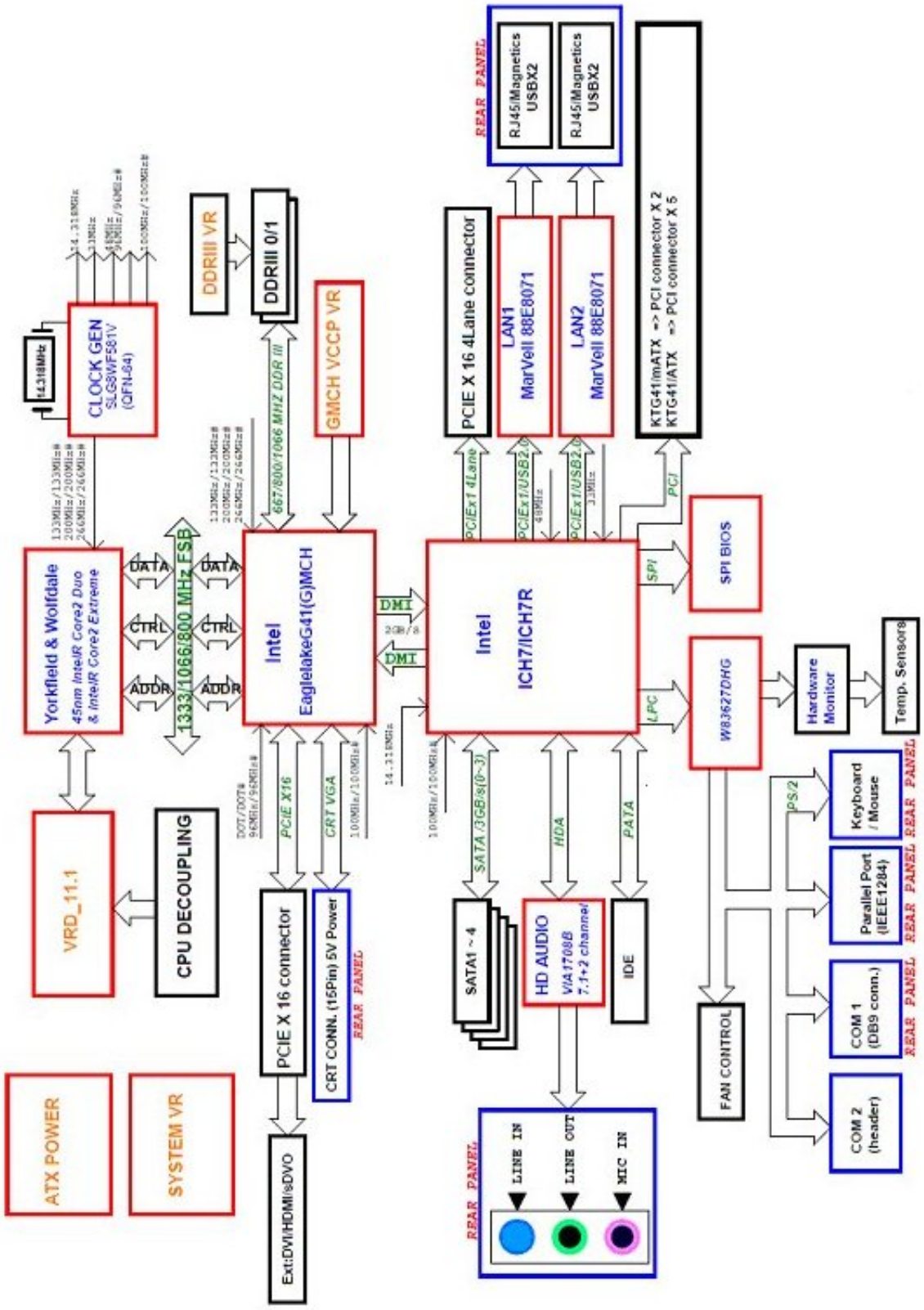
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Expansion Capabilities	• PCI Bus routed to PCI slots (PCI Local Bus Specification Revision 2.3) Two PCI slots (32 bits, 33 MHz, 5V compliant) • PCI-Express bus routed to PCI Express slots (PCI Express 1.0a) One PCI-Express x16 slot One PCI-Express x4 (in a x16 connector) slot • SMBus routed to FEATURE, PCI slot, PCI Express • LPC Bus routed to TPM connector • DDC Bus routed to CRT connector • 8 x GPIOs (General Purpose I/Os) routed to FEATURE connector
Hardware Monitor Subsystem	• Smart Fan control system, support Thermal® and Speed® cruise for three onboard Fan control connectors: FAN_CPU, FAN_SYS and FEATURE • Three thermal inputs: CPU die temperature, System temperature and External temperature input routed to FEATURE connector. (Precision +/- 3ºC) • Voltage monitoring • Intrusion detect input • SMI violations (BIOS) on HW monitor not supported. Supported by API (Windows).
Operating Systems Support	• WinXP • WinVista • Linux: Red Hat 5 U2, SuSe 10 SP2 (limitations may apply)
Environmental Conditions	**Operating**: 0°C – 55°C (forced cooling) and 10% - 90% relative humidity (non-condensing). It is the customer's responsibility to provide sufficient airflow around each of the components to keep them within allowed temperature range. **Storage**: -20°C – 70°C and 5% - 95% relative humidity (non-condensing) **Electro Static Discharge (ESD) / Radiated Emissions (EMI):** All Peripheral interfaces intended for connection to external equipment are ESD/ EMI protected. EN 61000-4-2:2000 ESD Immunity EN55022:1998 class B Generic Emission Standard. **Safety:** UL 60950-1:2003, 2nd Edition, 2007-03-27 CSA C22.2 No. 60950-1-07 2nd Edition, 2007-03 Product Category: Information Technology Equipment Including Electrical Business Equipment Product Category CCN: NWGQ2, NWGQ8 File number: E194252 **Theoretical MTBF:** 501.776 / 272.734 hours @ 40ºC / 60ºC **Restriction of Hazardous Substances (RoHS):** KTG41 is RoHS compliant. **Capacitor utilization:** No Tantalum capacitors on board Only Japanese brand Solid capacitors rated for 100ºC used on board
Battery	Exchangeable 3.0V Lithium battery for onboard Real Time Clock and CMOS RAM. Manufacturer Panasonic / Part-number CR-2032L/BN, CR2032NL/LE or CR-2032L/BE. Approximate 4-5 years retention. Current draw is 5-6µA when PSU is disconnected. **CAUTION: Danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.**

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2.2 System overview

The block diagram below shows the architecture and main components of the KTG41 board. The two key components on the board are the Intel® G41 and Intel® ICH7R Chipsets.



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2.3 Processor Support Table

The KTQ41/ATXu is designed to support the following LGA775 processors:

Intel® Core™ 2 Quad Processor

Intel® Core™ 2 Duo Processor

Intel® Pentium® Processor (2 cores)

Intel® Celeron®

In the following list the CPU Number in emphases means supported in according to Intel, but pt. not tested by Kontron.

Processor Brand	Clock Speed [GHz]	Bus Speed [MHz]	CPU Number	sSpec no.	Thermal Guideline [Watt]	Cache [MB]	Embedded
Intel® Core™2 Quad (Yorkfield)	3.00	1333	(Q9650)		95	12	-
	2.83	1333	(Q9550)		95	12	-
	2.83	1333	(Q9550S)		86.5	12	-
	2.66	1333	Q9450	SLAWR	95	12	-
	2.66	1333	Q9400	SLB6B	95	6	Yes
	2.66	1333	(Q9400S)		65	6	-
	2.50	1333	(Q9300)		95	6	-
	2.66	1333	(Q8400)		95	4	-
	2.66	1333	(Q8400S)		65	4	-
	2.50	1333	(Q8300)		95	4	-
	2.33	1333	(Q8200)		95	4	-
	2.33	1333	(Q8200S)		65	4	-
Intel® Core™ 2 Duo (Wolfdale)	3.33	1333	(E8600)		65	6	-
	3.16	1333	(E8500)		65	6	-
	3.00	1333	E8400	SLAPL	65	6	-
	3.00	1333	(E8400)	SLB9J	65	6	Yes
	2.83	1333	(E8300)		65	6	-
	2.66	1333	(E8200)		65	6	-
	2.66	1333	(E8190)		65	6	-
	3.06	1066	(E7600)		65	3	-
	2.93	1066	(E7500)		65	3	-
	2.80	1066	(E7400)		65	3	Yes
	2.66	1066	(E7300)		65	3	-
	2.53	1066	(E7200)		65	3	-
Intel® Core™ 2 Duo (Conroe)	3.00	1333	(E6850)		65	4	-
	2.66	1333	(E6750)		65	4	-
	2.66	1333	(E6700)		65	4	-
	2.40	1066	(E6600)		65	4	-
	2.33	1066	(E6550)		65	4	-
	2.33	1066	(E6540)		65	4	-
	2.13	1066	(E6420)		65	4	-
	2.13	1066	E6400	SLA97	65	2	Yes
	1.86	1066	(E6320)		65	4	-
	1.86	1066	(E6300)		65	2	-
	2.40	800	(E4600)		65	2	-
	2.20	800	(E4500)		65	2	-
	2.00	800	(E4400)		65	2	
	1.80	800	E4300	SL9TB	65	2	-
	1.80	800	(E4300)	SLA99	65	2	Yes

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Processor Brand	Clock Speed [GHz]	Bus Speed [MHz]	CPU Number	sSpec no.	Thermal Guideline [Watt]	Cache [MB]	Embedded
Intel® Pentium® (2 Cores) (Conroe)	2.70	800	(E5400)		65	2	-
	2.60	800	(E5300)		65	2	Yes
	2.50	800	(E5200)		65	2	-
	2.40	800	(E2220)		65	1	-
	2.20	800	(E2200)		65	1	-
	2.00	800	(E2180)		65	1	-
	1.80	800	E2160	SLA8Z	65	1	Yes
	1.60	800	(E2140)		65	1	-
Intel® Celeron® (Conroe)	2.40	800	(E1600)		65	0.5	-
	2.20	800	(E1500)		65	0.5	Yes
	2.00	800	(E1400)		65	0.5	-
	1.60	800	(E1200)		65	0.5	-
	2.00	800	(440)		35	0.5	Yes
	1.80	800	(430)		35	0.5	-
	1.60	800	(420)		35	0.5	-

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2.4 System Memory support

The KTG41 has two onboard DDR3 DIMM sockets and support the following memory features:

DDR3-800/1066 DIMM 240pin DRAM modules (PC3-6400/PC3-8500)

- 1.5V (only) 240-pin DDR3 SDRAM DIMMs with gold-plated contacts
- DDR3-800 (PC3-6400), DDR3-1066 (PC3-8500) SDRAM DIMMs
- DDR3-800/1066 DIMM with SPD timings supported
- Unbuffered, single-sided x8/x16 or double-sided x8/x16 DIMMs
- 4 GB maximum total system memory using 64-bit OS. (Shared Video Memory is withdrawn).
- 4 GB maximum total system memory using 32-bit OS. ~3GB is displayed in System Properties. (Shared Video Memory is withdrawn).
- Minimum total system memory: 512 MB
- Non-ECC DIMMs
- Serial Presence Detect

The installed DDR3 SDRAM should support the Serial Presence Detect (SPD) data structure. This allows the BIOS to read and configure the memory controller for optimal performance. If non-SPD memory is used, the BIOS will attempt to configure the memory settings, but performance and reliability may be impacted.

Memory Operating Frequencies
Regardless of the DIMM type used, the memory frequency will either be equal to or less than the processor system bus frequency. For example, if DDR3 800 memory is used with a 800 MHz system bus frequency processor, the memory clock will operate at 400 MHz. The table below lists the resulting operating memory frequencies based on the combination of DIMMs and processors.

DIMM Type	Processor system bus frequency [MHz]	Memory Data transfers [Mill/s]	Resulting memory clock frequency [MHz]	Module name	Peak transfer rate [MB/s]
DDR3 800	800	800	400	PC3-6400	6400
DDR3 800	1066	800	400	PC3-6400	6400
DDR3 800	1333	800	400	PC3-6400	6400
DDR3 1066	800	1066	400	PC3-8500	8533
DDR3 1066	1066	1066	533	PC3-8500	8533
DDR3 1066	1333	1066	533	PC3-8500	8533

Note: Kontron offers the following memory modules:
- P/N 1028-6891, DDR3-RAM, **1GB**, 240p, 800MHZ, PC3-8500, DIMM
- P/N 1028-6892, DDR3-RAM, **2GB**, 240p, 800MHZ, PC3-8500, DIMM

Memory Configurations

1. Asymmetric mode (Single channel). This mode is equivalent to single channel bandwidth operation. This mode is used when only one DIMM is installed or two DIMMs with different memory capacities are installed. Technology can vary from one DIMM to the other but if different speed is used, the slowest memory timing will be used.

2. Interleaved mode (Dual channel). This mode offers the highest throughput. Dual channel mode is enabled when two DIMM with same memory capacity are installed. Technology can vary from one DIMM to the other but if different speed is used, the slowest memory timing will be used.



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2.5 KTG41 Graphics Subsystem

The KTG41 use the Intel G41 chipset for the graphical control. This chipset contains two separate, mutually exclusive graphics options. Either the GMA X4500 graphics controller (contained within the AC82G41 GMCH) is used, or a PCI Express x16 add-in card can be used. When a PCI Expressx16 add-in card is installed, the GMA X4500 graphics controller is disabled.

2.5.1 Intel® GMA X4500

Features of the Intel GMA (Graphic Media Accelerator) X4500 graphics controller includes:

- High quality graphics engine supporting
    - DX10* and OpenGL* 2.0 compliant
    - Core frequency of 400 MHz
    - 1.6 GP/s pixel rate
    - High-Quality 3D Setup and Render Engine
    - High-Quality Texture Engine
    - 3D Graphics Rendering Enhancements
    - 2D Graphics
    - Video Overlay
    - Multiple Overlay Functionality
- Analogue Display (CRT)
    - 350 MHz Integrated 24-bit RAMDAC
    - Up to 2048x1536 @ 75 Hz refresh
    - Hardware Colour Cursor Support
    - DDC2B Compliant Interface
- Digital Display
    - SDVO ports in single mode supported
    - 200 MHz dot clock on each 12-bit interface
    - Flat panels up to 2048x1536 @ 60 Hz or digital CRT/HDTV at 1400x1050 @ 85 Hz
    - Dual independent display options with digital display
    - Multiplexed digital display channels (supported with ADD2 Card)
    - Supports TMDS transmitters or TV-Out encoders
    - ADD2/MEC card uses PCI Express graphics x16 connector
    - Two channels multiplexed with PCI Express* Graphics port
    - Supports Hot-Plug and Display
- Dynamic Video Memory Technology (DVMT 5.0) support up to 352 MB

2.5.2 DVMT 5.0 support

DVMT enables enhanced graphics and memory performance through highly efficient memory utilization. DVMT ensures the most efficient use of available system memory for maximum 2-D/3-D graphics performance. Up to 352 MB of system memory can be allocated to DVMT on systems that have 512 MB or more of total system memory installed. DVMT returns system memory back to the operating system when the additional system memory is no longer required by the graphics subsystem.
DVMT will always use a minimal fixed portion of system physical memory (as set in the BIOS Setup) for compatibility with legacy applications. An example of this would be when using VGA graphics under DOS. Once loaded, the operating system and graphics drivers allocate additional system memory to the graphics buffer as needed for performing graphics functions.

IMPORTANT: The use of DVMT requires driver support by the operating system.

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2.5.3 ADD2 (Advanced Digital Display) card support

The KTQ45 board routes two multiplexed SDVO ports that are each capable of driving up to a 200 MHz pixel clock to the PCI Express x16 connector. The SDVO ports can be paired for a dual channel configuration to support up to a 400 MHz pixel clock. When an ADD2 card is detected, the Intel GMA X4500 graphics controller is enabled and the PCI Express x16 connector is configured for SDVO mode. SDVO mode enables the SDVO ports to be accessed by the ADD2 card. An ADD2 card can either be configured to support simultaneous display with the primary VGA display or can be configured to support dual independent display as an extended desktop configuration with different colour depths and resolutions.

ADD2 cards can be designed to support the following configurations:

- TV-Out (composite video)
- Transition Minimized Differential Signalling (TMDS) for DVI 1.0
- Low Voltage Differential Signalling (LVDS)
- Single device operating in dual channel mode
- VGA output
- HDTV output
- HDMI/UDI support (when used with the HD Audio Link)

Currently Kontron plans the availability of the following ADD2 cards

- P/N 820953, ADD2-LVDS
- P/N 820950, ADD2-Dual LVDS
- P/N 820951, ADD2-Dual Internal DVI
- P/N 820952, ADD2-Dual DVI

Please visit the Kontron website (www.kontron.com) for details.

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2.6 Power Consumption

In order to ensure safe operation of the board, the ATX power supply must monitor the supply voltage and shut down if the supplies are out of range – refer to the hardware manual for actual power specification.

The KTQ45/Flex board is powered through the ATX connector and the additional 12V separate supply for CPU as specified in the ATX specification; besides this the power supplied to the board must be within the ATX specification.

The requirements to the supply voltages are as follows:

Supply	Min	Max	Note
VCC3.3	3.168V	3.432V	Should be ±4% for compliance with the ATX specification
Vcc	4.75V	5.25V	Should be ±5% for compliance with the ATX specification. Should be minimum 5.00V measured at USB connectors in order to meet the requirements of USB standard .
+12V	11.4V	12.6V	Should be ±5% for compliance with the ATX specification
–12V	–13.2V	–10.8V	Should be ±10% for compliance with the ATX specification
-5V	-5,50V	-4.5V	Not required for the KTQ45 boards
5VSB	4.75V	5.25V	Should be ±5% for compliance with the ATX specification

Static Power Consumption

The power consumption of the KTQ45/ATXu Board is measured under:

1- DOS, idle, mean
2- WindowsXP, Running 3DMARK 2001 & 2 x CPU BURN, mean
3- S1, mean
4- S3, mean
5- S4, mean

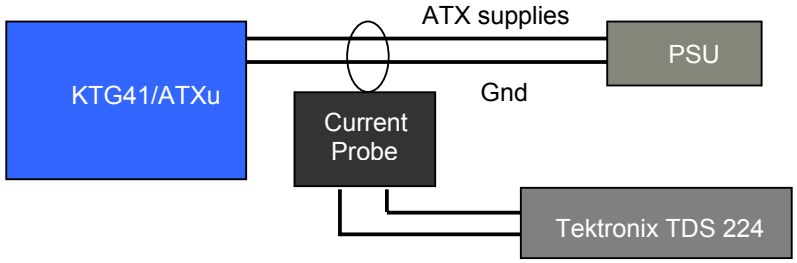
Test system configuration

Test system configuration

The following items were used in the test setup:

1. KTG41/ATXu board mounted w/ 3.00GHz (E8400) Core Duo & 1GB Samsung 1Rx8 PC3-10600U-09-00-A0 1,5V DDR3 Ram
2. 12V active cooler
3. PS/2 keyboard & mouse (Mouse:Genius Netscroll+ Keyboard:ACK-595)
4. CRT (Nokia 477Pro)
5. HD (Seagate Barracuda 7200.10 160 GB)
6. ATX PSU (OCZ-420ADJ)
7. Tektronix TDS 224, P6345 probes
8. Fluke Current Probe 80i-100S AC/DC

Test setup



Note: The Power consumption of CRT, HD and Fan is not included.

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DOS Idle, Mean, No external load		
Supply	Current draw	Power consumption
+12V	2.12A	25.44W
+5V	0.22A	1.10W
+3V3	2.50A	8.25W
-12V	-	0W
5VSB	-	0W
Total		34.79W

Windows XP, mean 3DMARK2001 (Game 1 – Car Chase test) & 2 x CPUBURN		
Supply	Current draw	Power consumption
+12V	3.21A	38.52W
+5V	3.49A	17.45W
+3V3	0.24A	0.79W
-12V	0.00A	0W
5VSB	0.00A	0W
Total		56.76W

S1 Mode, Mean, No external load		
Supply	Current draw	Power consumption
+12V	1.14A	13.68W
+5V	0.15A	0.75W
+3V3	2.02A	6.66W
-12V	0.00A	0W
5VSB	0.00A	0W
Total		21.09W

S3 Mode, Mean, No external load		
Supply	Current draw	Power consumption
+12V	0.00A	0W
+5V	0.00A	0W
+3V3	0.00A	0W
-12V	0.00A	0W
5VSB	0.49A	2.45W
Total		2.45W

S4 Mode, Mean, No external load		
Supply	Current draw	Power consumption
+12V	0.00A	0W
+5V	0.00A	0W
+3V3	0.00A	0W
-12V	0.00A	0W
5VSB	0.44A	2.20W
Total		2.20W

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3 Connector Definitions

The following sections provide pin definitions and detailed description of all on-board connectors.

The connector definitions follow the following notation:

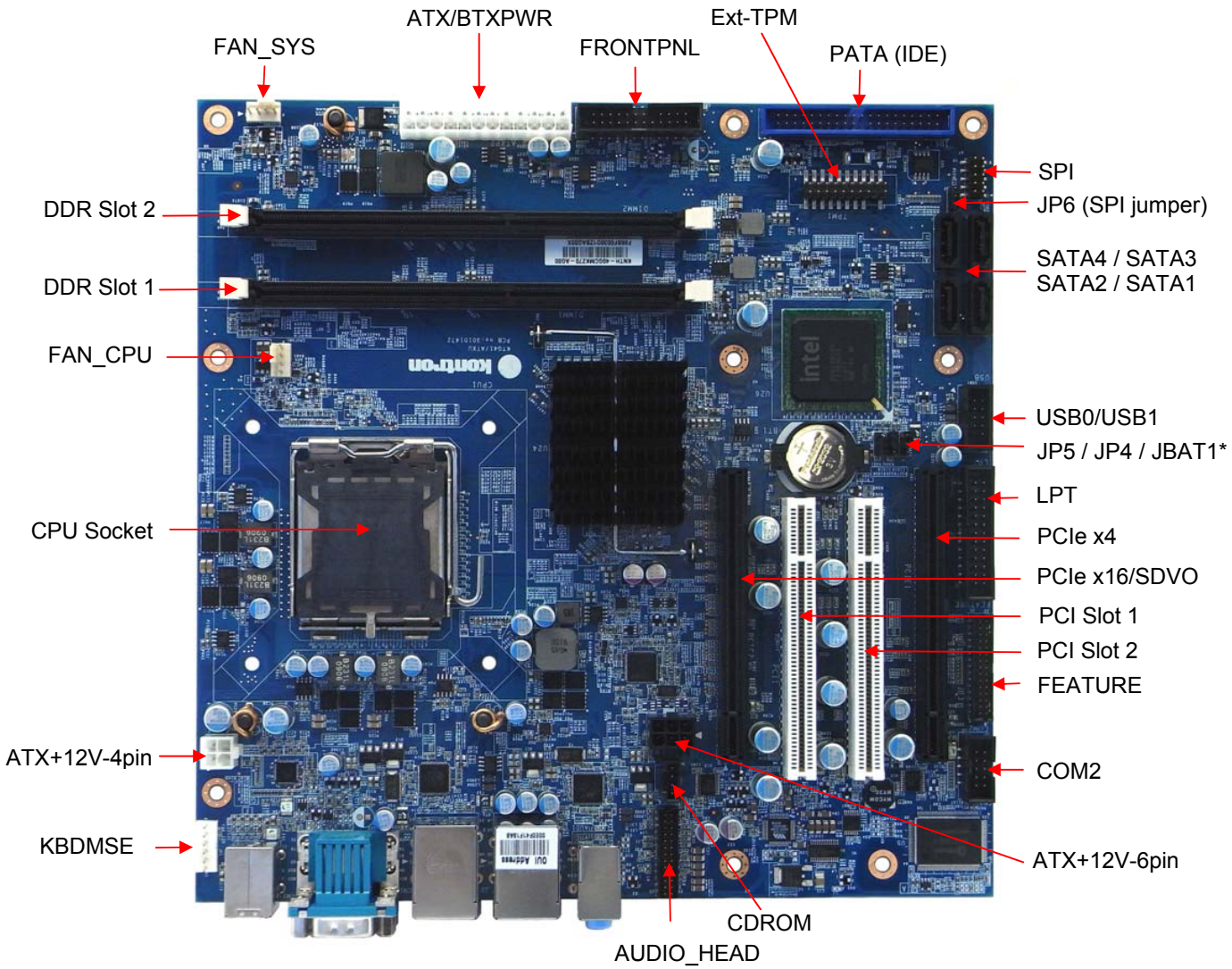
Column name	Description
Pin	Shows the pin-numbers in the connector. The graphical layout of the connector definition tables is made similar to the physical connectors.
Signal	The mnemonic name of the signal at the current pin. The notation “XX#” states that the signal “XX” is active low.
Type	AI : Analogue Input. AO : Analogue Output. I : Input, TTL compatible if nothing else stated. IO : Input / Output. TTL compatible if nothing else stated. IOT : Bi-directional tristate IO pin. IS : Schmitt-trigger input, TTL compatible. IOC : Input / open-collector Output, TTL compatible. NC : Pin not connected. O : Output, TTL compatible. OC : Output, open-collector or open-drain, TTL compatible. OT : Output with tri-state capability, TTL compatible. LVDS: Low Voltage Differential Signal. PWR : Power supply or ground reference pins.
	Ioh: Typical current in mA flowing out of an output pin through a grounded load, while the output voltage is > 2.4 V DC (if nothing else stated). Iol: Typical current in mA flowing into an output pin from a VCC connected load, while the output voltage is < 0.4 V DC (if nothing else stated).
Pull U/D	On-board pull-up or pull-down resistors on input pins or open-collector output pins.
Note	Special remarks concerning the signal.

The abbreviation *TBD* is used for specifications which are not available yet or which are not sufficiently specified by the component vendors.

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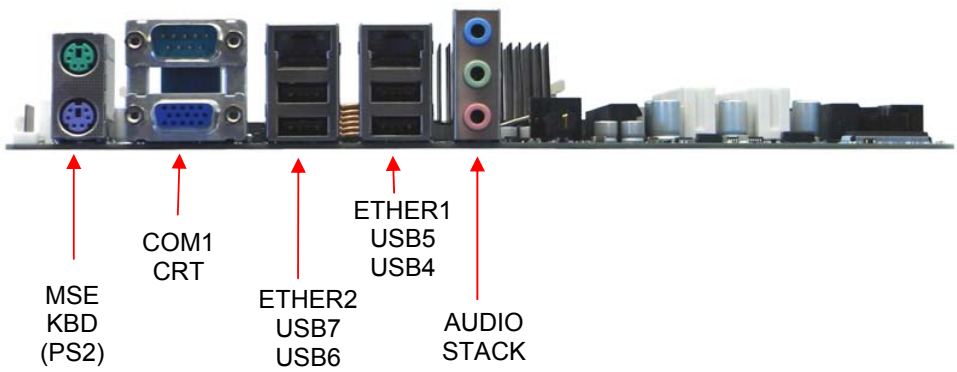
3.1 Connector layout

3.1.1 KTG41 - Top Side View



* JP5 / JP4 used for BIOS boot selection
(only for manufacture purpose)
JBAT1 used for Clear CMOS

3.1.2 KTG41 - IO Bracket area



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3.2 Power Connector (ATX/BTXPWR)

The KTG41 is designed to be supplied from a standard ATX or BTX power supply.

ATX/ BTX Power Connector:

Note	Type	Signal	PIN		Signal	Type	Note
	PWR	3V3	12	24	GND	PWR	
	PWR	+12V	11	23	5V	PWR	
	PWR	+12V	10	22	5V	PWR	
	PWR	SB5V	9	21	5V	PWR	
	I	P_OK	8	20	-5V	PWR	1
	PWR	GND	7	19	GND	PWR	
	PWR	5V	6	18	GND	PWR	
	PWR	GND	5	17	GND	PWR	
	PWR	5V	4	16	PSON#	OC	
	PWR	GND	3	15	GND	PWR	
	PWR	3V3	2	14	-12V	PWR	
	PWR	3V3	1	13	3V3	PWR	

Note 1: -5V supply is not used onboard.
Note: Use of BTX supply not required for operation, but may be required to drive high-power PCIe cards. See chapter “Power Consumption” regarding input tolerances on 3.3V, 5V, SB5V, +12 and -12V (also refer to ATX specification version 2.2).

ATX+12V-6pin Power Connector (same net as +12V in ATX/BTX Power connector):

Note	Type	Signal	PIN		Signal	Type	Note
1	PWR	+12V	1	4	GND	PWR	
1	PWR	+12V	2	5	GND	PWR	
	PWR	+12V	3	6	GND	PWR	

ATX+12V-4pin Power Connector:

Note	Type	Signal	PIN		Signal	Type	Note
1	PWR	+12V	1	3	GND	PWR	
1	PWR	+12V	2	4	GND	PWR	

Note 1: Use of the 4-pin ATX+12V Power Connector is required for operation of the KTG41.

Signal	Description
P_OK	P_OK is a power good signal and should be asserted high by the power supply to indicate that the +5VDC and +3.3VDC outputs are above the undervoltage thresholds of the power supply. When this signal is asserted high, there should be sufficient energy stored by the converter to guarantee continuous power operation within specification. Conversely, when the output voltages fall below the undervoltage threshold, or when mains power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, P_OK should be de-asserted to a low state. The recommended electrical and timing characteristics of the P_OK (PWR_OK) signal are provided in the *ATX12V Power SupplyDesign Guide*. It is strongly recommended to use an ATX or BTX supply with the KTG41, in order to implement the supervision of the 5V and 3V3 supplies. These supplies are not supervised onboard the KTG41.
PS_ON#	Active low open drain signal from the board to the power supply to turn on the power supply outputs. Signal must be pulled high by the power supply.

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3.3 Keyboard and Mouse connectors

Attachment of a keyboard or PS/2 mouse adapter can be done through the stacked PS/2 mouse and keyboard connector (MSE & KBD).

Both interfaces utilize open-drain signalling with on-board pull-up.

The PS/2 mouse and keyboard is supplied from SB5V when in standby mode in order to enable keyboard or mouse activity to bring the system out from power saving states. The supply is provided through a 1.1A resettable fuse.

3.3.1 MINI-DIN Keyboard and Mouse Connector (KBD)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	-	NC	6 5	MSCLK	IOC	TBD	2K7	
	-	-	PWR	5V/SB5V	4 3	GND	PWR	-	-	
	-	-	-	NC	2 1	MSDAT	IOC	TBD	2K7	
	-	-	-	NC	6 5	KBDCLK	IOC	TBD	2K7	
	-	-	PWR	5V/SB5V	4 3	GND	PWR	-	-	
	-	-	-	NC	2 1	KBDDAT	IOC	TBD	2K7	

Signal Description – Keyboard & and mouse Connector (MSE & KBD), see below.

3.3.2 Keyboard and Mouse pinrow Connector (KBDMSE)

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	KBDCLK	IOC	TBD	2K7	
2	KBDDAT	IOC	TBD	2K7	
3	MSCLK	IOC	TBD	2K7	
4	MSDAT	IOC	TBD	2K7	
5	5V/SB5V	PWR	-	-	
6	GND	PWR	-	-	

Signal Description – Keyboard & and mouse Connector (KBDMSE).

Signal	Description
MSCLK	Bi-directional clock signal used to strobe data/commands from/to the PS/2 mouse.
MSDAT	Bi-directional serial data line used to transfer data from or commands to the PS/2 mouse.
KDBCLK	Bi-directional clock signal used to strobe data/commands from/to the PC-AT keyboard.
KBDDAT	Bi-directional serial data line used to transfer data from or commands to the PC-AT keyboard.

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3.4 Display connector

The KTG41 provides onboard Analogue CRT interface. Additionally the KTG41 provides support for ADD2 cards through the onboard PCI Express x16 connector, with extension capability for support of DVI, LVDS, VGA, HDMI/UDI, TV-Out, etc.
If a PCI Express x16 Graphics add-on card is used, the onboard Graphics controller (GMA X4500) is disabled.

3.4.1 CRT Connector (CRT)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
						6	GND	PWR	-	-	
	/75R	*	A0	RED	1	11	NC	-	-	-	
						7	GND	PWR	-	-	
	/75R	*	A0	GREEN	2	12	DDCDAT	IO	TBD	2K2	
						8	GND	PWR	-	-	
	/75R	*	A0	BLUE	3	13	HSYNC	O	TBD		
						9	5V	PWR	-	-	1
	-	-	-	NC	4	14	VSYNC	O	TBD		
						10	GND	PWR	-	-	
	-	-	PWR	GND	5	15	DDCCLK	IO	TBD	2K2	

Signal Description - CRT Connector:

Pin	Signal	Description
1	RED	Analogue output carrying the red colour signal to the CRT. For 75 Ohm cable impedance.
2	GREEN	Analogue output carrying the green colour signal to the CRT. For 75 Ohm cable impedance.
3	BLUE	Analogue output carrying the blue colour signal to the CRT. For 75 Ohm cable impedance.
4	NC	No Connection
5-8	GND	
9	5V	This 5V supply is fused by a 1.1A resettable fuse.
10	GND	
11	NC	No Connection
12	DDCDAT	Display Data Channel Data. Used as data signal to/from monitors with DDC interface.
13	HSYNC	CRT horizontal synchronization output.
14	VSYNC	CRT vertical synchronization output.
15	DDCCLK	Display Data Channel Clock. Used as clock signal to/from monitors with DDC interface.

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3.5 PCI-Express connectors

The KTG41 supports one 16-lane (x16) PCI Express port and one 4-lane PCI Express (x16) port.

The 16-lane (x16) PCI Express can be used for external PCI Express graphics card. It is located nearest the CPU.

The PCI Express port is compliant to the PCI Express Base Specification revision 1.1. The x16 port operates at a frequency of 2.5 Gbit/s on each lane while employing 8b/10b encoding; the port supports a maximum theoretical bandwidth of 40 Gbit/s in each direction.

The PCI Express (x16) interface is multiplexed with the SDVO ports.

The 4-lane (x4) PCI Express port is mechanically an x16 port and electrically an x4 port. It is located farthest away from CPU.

3.5.1 PCI-Express x16/SDVO Connector (PCIe x16/SDVO)

Note	Type	Signal	PIN		Signal	Type	Note
		+12V	B1	A1	NC		
		+12V	B2	A2	+12V		
		+12V	B3	A3	+12V		
		GND	B4	A4	GND		
		SMB_CLK	B5	A5	NC		
		SMB_DATA	B6	A6	NC		
		GND	B7	A7	NC		
		+3V3	B8	A8	NC		
		NC	B9	A9	+3V3		
		SB3V3	B10	A10	+3V3		
		WAKE#	B11	A11	RST#		
		NC	B12	A12	GND		
		GND	B13	A13	PCIE_x16 CLK		
		PEG_TXP[15]/SDVOB_RED	B14	A14	PCIE_x16 CLK#		
		PEG_TXN[15]/SDVOB_RED#	B15	A15	GND		
		GND	B16	A16	PEG_RXP[15]/SDVO_TVCLKIN		
		SDVO_CTRLCLK	B17	A17	PEG_RXN[15] / SDVO_TVCLKIN#		
		GND	B18	A18	GND		
		PEG_TXP[14]/SDVOB_GREEN	B19	A19	NC		
		PEG_TXN[14]/SDVOB_GREEN#	B20	A20	GND		
		GND	B21	A21	PEG_RXP[14]/SDVOB_INT		
		GND	B22	A22	PEG_RXN[14]/SDVOB_INT#		
		PEG_TXP[13]/SDVOB_BLUE	B23	A23	GND		
		PEG_TXN[13]/SDVOB_BLUE#	B24	A24	GND		
		GND	B25	A25	PEG_RXP[13]/SDVO_FLDSTALL		
		GND	B26	A26	PEG_RXN[13]/SDVO_FLDSTALL#		
		PEG_TXP[12]/SDVOB_CLKP	B27	A27	GND		
		PEG_TXN[12]/SDVOB_CLKN	B28	A28	GND		
		GND	B29	A29	PEG_RXP[12]		
		NC	B30	A30	PEG_RXN[12]		
		SDVO_CTRLDATA	B31	A31	GND		
		GND	B32	A32	NC		
		PEG_TXP[11]/SDVOC_RED	B33	A33	NC		
		PEG_TXN[11]/SDVOC_RED#	B34	A34	GND		
		GND	B35	A35	PEG_RXP[11]		
		GND	B36	A36	PEG_RXN[11]		
		PEG_TXP[10]/SDVOC_GREEN	B37	A37	GND		
		PEG_TXN[10]/SDVOC_GREEN#	B38	A38	GND		
		GND	B39	A39	PEG_RXP[10]/SDVOC_INT		

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		GND	B40	A40	PEG_RXN[10]/SDVOC_INT#		
		PEG_TXP[9]/SDVOC_BLUE	B41	A41	GND		
		PEG_TXN[9]/SDVOC_BLUE#	B42	A42	GND		
		GND	B43	A43	PEG_RXP[9]		
		GND	B44	A44	PEG_RXN[9]		
		PEG_TXP[8]/SDVOC_CLKN	B45	A45	GND		
		PEG_TXN[8]/SDVOC_CLKP	B46	A46	GND		
		GND	B47	A47	PEG_RXP[8]		
		PRSNT#2	B48	A48	PEG_RXN[8]		
		GND	B49	A49	GND		
		PEG_TXP[7]	B50	A50	NC		
		PEG_TXN[7]	B51	A51	GND		
		GND	B52	A52	PEG_RXP[7]		
		GND	B53	A53	PEG_RXN[7]		
		PEG_TXP[6]	B54	A54	GND		
		PEG_TXN[6]	B55	A55	GND		
		GND	B56	A56	PEG_RXP[6]		
		GND	B57	A57	PEG_RXN[6]		
		PEG_TXP[5]	B58	A58	GND		
		PEG_TXN[5]	B59	A59	GND		
		GND	B60	A60	PEG_RXP[5]		
		GND	B61	A61	PEG_RXN[5]		
		PEG_TXP[4]	B62	A62	GND		
		PEG_TXN[4]	B63	A63	GND		
		GND	B64	A64	PEG_RXP[4]		
		GND	B65	A65	PEG_RXN[4]		
		PEG_TXP[3]	B66	A66	GND		
		PEG_TXN[3]	B67	A67	GND		
		GND	B68	A68	PEG_RXP[3]		
		GND	B69	A69	PEG_RXN[3]		
		PEG_TXP[2]	B70	A70	GND		
		PEG_TXN[2]	B71	A71	GND		
		GND	B72	A72	PEG_RXP[2]		
		GND	B73	A73	PEG_RXN[2]		
		PEG_TXP[1]	B74	A74	GND		
		PEG_TXN[1]	B75	A75	GND		
		GND	B76	A76	PEG_RXP[1]		
		GND	B77	A77	PEG_RXN[1]		
		PEG_TXP[0]	B78	A78	GND		
		PEG_TXN[0]	B79	A79	GND		
		GND	B80	A80	PEG_RXP[0]		
		NC	B81	A81	PEG_RXN[0]		
		NC	B82	A82	GND		

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3.5.2 PCI-Express x4 Connector (PCIe x4)

Note	Type	Signal	PIN		Signal	Type	Note
		+12V	B1	A1	NC		
		+12V	B2	A2	+12V		
		+12V	B3	A3	+12V		
		GND	B4	A4	GND		
		SMB_CLK	B5	A5	NC		
		SMB_DATA	B6	A6	NC		
		GND	B7	A7	NC		
		+3V3	B8	A8	NC		
		NC	B9	A9	+3V3		
		SB3V3	B10	A10	+3V3		
		WAKE#	B11	A11	RST#		
		NC	B12	A12	GND		
		GND	B13	A13	PCIE_x4 CLK		
		PCIE_TXP[1]	B14	A14	PCIE_x4 CLK#		
		PCIE_TXN[1]	B15	A15	GND		
		GND	B16	A16	PCIE_RXP[1]		
		NC	B17	A17	PCIE_RXN[1]		
		GND	B18	A18	GND		
		PCIE_TXP[2]	B19	A19	NC		
		PCIE_TXN[2]	B20	A20	GND		
		GND	B21	A21	PCIE_RXP[2]		
		GND	B22	A22	PCIE_RXN[2]		
		PCIE_TXP[3]	B23	A23	GND		
		PCIE_TXN[3]	B24	A24	GND		
		GND	B25	A25	PCIE_RXP[3]		
		GND	B26	A26	PCIE_RXN[3]		
		PCIE_TXP[4]	B27	A27	GND		
		PCIE_TXN[4]	B28	A28	GND		
		GND	B29	A29	PCIE_RXP[4]		
		NC	B30	A30	PCIE_RXN[4]		
		NC	B31	A31	GND		
		GND	B32	A32	NC		
		NC	B33	A33	NC		
		NC	B34	A34	GND		
		GND	B35	A35	NC		
		GND	B36	A36	NC		
		NC	B37	A37	GND		
		NC	B38	A38	GND		
		GND	B39	A39	NC		
		GND	B40	A40	NC		
		NC	B41	A41	GND		
		NC	B42	A42	GND		
		GND	B43	A43	NC		
		GND	B44	A44	NC		
		NC	B45	A45	GND		
		NC	B46	A46	GND		
		GND	B47	A47	NC		
		NC	B48	A48	NC		
		GND	B49	A49	GND		
		NC	B50	A50	NC		
		NC	B51	A51	GND		
		GND	B52	A52	NC		
		GND	B53	A53	NC		
		NC	B54	A54	GND		
		NC	B55	A55	GND		
		GND	B56	A56	NC		
		GND	B57	A57	NC		
		NC	B58	A58	GND		
		NC	B59	A59	GND		

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		GND	B60	A60	NC		
		GND	B61	A61	NC		
		NC	B62	A62	GND		
		NC	B63	A63	GND		
		GND	B64	A64	NC		
		GND	B65	A65	NC		
		NC	B66	A66	GND		
		NC	B67	A67	GND		
		GND	B68	A68	NC		
		GND	B69	A69	NC		
		NC	B70	A70	GND		
		NC	B71	A71	GND		
		GND	B72	A72	NC		
		GND	B73	A73	NC		
		NC	B74	A74	GND		
		NC	B75	A75	GND		
		GND	B76	A76	NC		
		GND	B77	A77	NC		
		NC	B78	A78	GND		
		NC	B79	A79	GND		
		GND	B80	A80	NC		
		NC	B81	A81	NC		
		NC	B82	A82	GND		

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3.6 IDE Hard Disk Connector (PATA)

The IDE (40 pin IDC) connector can be used for connection of two primary IDE drives like standard 3½" hard disks or CD-ROM drives.

The parallel ATA harddisk controller is shared between the PATA connector and the Hyperflash adapter (Accessory). Hyperflash adapter and PATA disk are not supported at the same time.

The hard disk controllers support Bus master IDE, ultra DMA 33/66/100 MHz and standard operation modes. For support of ultra DMA 33/66/100 MHz, an 80 wire cable is required.

Note	Pull U/D	Ioh/ Iol	Type	Signal	PIN		Signal	Type	Ioh/ Iol	Pull U/D	Note
	-	TBD	O	RESET_P#	1	2	GND	PWR	-	-	
	-	TBD	IO	DA7	3	4	DA8	IO	TBD	-	
	-	TBD	IO	DA6	5	6	DA9	IO	TBD	-	
	-	TBD	IO	DA5	7	8	DA10	IO	TBD	-	
	-	TBD	IO	DA4	9	10	DA11	IO	TBD	-	
	-	TBD	IO	DA3	11	12	DA12	IO	TBD	-	
	-	TBD	IO	DA2	13	14	DA13	IO	TBD	-	
	-	TBD	IO	DA1	15	16	DA14	IO	TBD	-	
	-	TBD	IO	DA0	17	18	DA15	IO	TBD	-	
	-	-	PWR	GND	19	20	KEY	-	-	-	
	-	-	I	DDRQA	21	22	GND	PWR	-	-	
	-	TBD	O	IOWA#	23	24	GND	PWR	-	-	
	-	TBD	O	IORA#	25	26	GND	PWR	-	-	
	4K7	-	I	IORDYA	27	28	GND	PWR	-	-	
	-	-	O	DDACKA#	29	30	GND	PWR	-	-	
	10K	-	I	HDIRQA	31	32	NC	-	-	-	
	-	TBD	O	DAA1	33	34	CBLIDA#	I	-		
	-	TBD	O	DAA0	35	36	DAA2	O	TBD	-	
	-	TBD	O	HDCSA0#	37	38	HDCSA1#	O	TBD	-	
	-	-	I	HDACTA#	39	40	GND	PWR	-	-	

Signal	Description
DAA2..0	Address lines, used to address the I/O registers in the IDE hard disk.
HDCSA1..0#	Hard Disk Chip-Select. HDCS0# selects the primary hard disk.
DA15..8	High part of data bus.
DA7..0	Low part of data bus.
IORA#	I/O Read.
IOWA#	I/O Write.
IORDYA#	This signal may be driven by the hard disk to extend the current I/O cycle.
RESETA#	Reset signal to the hard disk.
HDIRQA	Interrupt line from hard disk.
CBLIDA	This input signal (CaBLe ID) is used to detect the type of attached cable: 80-wire cable when low input and 40-wire cable when 5V via 10Kohm (pull-up resistor).
DDREQA	Disk DMA Request might be driven by the IDE hard disk to request bus master access to the PCI bus. The signal is used in conjunction with the PCI bus master IDE function and is not associated with any PC-AT bus compatible DMA channel.
DDACKA#	Disk DMA Acknowledge. Active low signal grants IDE bus master access to the PCI bus.
HDACTA#	Signal from hard disk indicating hard disk activity. The signal level depends on the hard disk type, normally active low. The signals from primary and secondary controller are routed together through diodes and passed to the connector FEATURE.

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3.7 Serial ATA Hard Disk interface

The KTG41 has integrated SATA Host controller that supports independent DMA operation on four SATA (Serial ATA) ports for connection of one device per SATA connector. The SATA ports supports data transfer rates of up to 3.0Gbit/s (300MB/s) and the SATA controller supports AHCI mode and has integrated RAID functionality with support for RAID modes 0, 1, 5 and 10 (Linux O/S only support for RAID 0 and 1).

For compatibility, the underlying Serial ATA functionality is transparent to the operating system. The Serial ATA controller can operate in both legacy and native modes. In legacy mode, standard IDE I/O and IRQ resources are assigned (IRQ 14 and 15). In Native mode, standard PCI Conventional bus resource steering is used. Native mode is the preferred mode for configurations using the Windows XP and Windows Vista operating systems.

The KTG41 supports the following RAID (Redundant Array of Independent Drives) levels:

- RAID 0 - data striping
- RAID 1 - data mirroring
- RAID 0+1 (or RAID 10) - data striping and mirroring
- RAID 5 - distributed parity
- Matrix 2+2

Limitations depending on Target Operating System apply.

3.7.1 SATA Hard Disk Connector (SATA1, SATA2, SATA3, SATA4)

SATA:

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	GND	PWR	-	-	
2	SATA* TX+				
3	SATA* TX-				
4	GND	PWR	-	-	
5	SATA* RX-				
6	SATA* RX+				
7	GND	PWR	-	-	

The signals used for the primary Serial ATA hard disk interface are the following:

Signal	Description
SATA* RX+ SATA* RX-	Host transmitter differential signal pair
SATA* TX+ SATA* TX-	Host receiver differential signal pair

"*" specifies 1, 2, 3, 4 depending on SATA port.

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3.8 Printer Port Connector (LPT)

The signal definition in standard printer port mode is as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	2K2	(24)/24	OC(O)	STB#	1	2	AFD#	OC(O)	(24)/24	2K2	
	2K2	24/24	IO	PD0	3	4	ERR#	I	-	2K2	
	2K2	24/24	IO	PD1	5	6	INIT#	OC(O)	(24)/24	2K2	
	2K2	24/24	IO	PD2	7	8	SLIN#	OC(O)	(24)/24	2K2	
	2K2	24/24	IO	PD3	9	10	GND	PWR	-	-	
	2K2	24/24	IO	PD4	11	12	GND	PWR	-	-	
	2K2	24/24	IO	PD5	13	14	GND	PWR	-	-	
	2K2	24/24	IO	PD6	15	16	GND	PWR	-	-	
	2K2	24/24	IO	PD7	17	18	GND	PWR	-	-	
	2K2	-	I	ACK#	19	20	GND	PWR	-	-	
	2K2	-	I	BUSY	21	22	GND	PWR	-	-	
	2K2	-	I	PE	23	24	GND	PWR	-	-	
	2K2	-	I	SLCT	25	26	GND	PWR	-	-	

The definition of the signals in standard Centronics mode (SPP) with a printer attached is as follows:

Signal	Description
PD7..0	Parallel data bus from PC board to printer. The data lines are able to operate in PS/2 compatible bi-directional mode.
SLIN#	Signal to select the printer sent from CPU board to printer.
SLCT	Signal from printer to indicate that the printer is selected.
STB#	This signal indicates to the printer that data at PD7..0 are valid.
BUSY	Signal from printer indicating that the printer cannot accept further data.
ACK#	Signal from printer indicating that the printer has received the data and is ready to accept further data.
INIT#	This active low output initializes (resets) the printer.
AFD#	This active low output causes the printer to add a line feed after each line printed.
ERR#	Signal from printer indicating that an error has been detected.
PE#	Signal from printer indicating that the printer is out of paper.

The printer port additionally supports operation in the EPP and ECP mode.

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3.9 Serial Ports

Two RS232 serial ports are available on the KTG41.

The typical definition of the signals in the COM ports is as follows:

Signal	Description
TxD	Transmitted Data, sends serial data to the communications link. The signal is set to the marking state (-12V) on hardware reset when the transmitter is empty or when loop mode operation is initiated.
RxD	Received Data, receives serial data from the communications link.
DTR	Data Terminal Ready, indicates to the modem or data set that the on-board UART is ready to establish a communication link.
DSR	Data Set Ready, indicates that the modem or data set is ready to establish a communications link.
RTS	Request To Send, indicates to the modem or data set that the on-board UART is ready to exchange data.
CTS	Clear To Send, indicates that the modem or data set is ready to exchange data.
DCD	Data Carrier Detect, indicates that the modem or data set has detected the data carrier.
RI	Ring Indicator, indicates that the modem has received a ringing signal from the telephone line.

The connector pinout for each operation mode is defined in the following sections.

3.9.1 COM1 Connectors

COM1 is RS232 port available in the IO Bracket area. The pinout of Serial ports Com1 is as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	GND	5					
					9	RI	I	-	/5K	
	-		O	DTR	4					
					8	CTS	I	-	/5K	
	-		O	TxD	3					
					7	RTS	O		-	
	/5K	-	I	RxD	2					
					6	DSR	I	-	/5K	
	/5K	-	I	DCD	1					

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3.9.2 COM2 Header Connectors

The pinout of Serial ports COM2 is as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
		-	I	DCD	1	2	DSR	I	-		
		-	I	RxD	3	4	RTS	O		-	
	-		O	TxD	5	6	CTS	I	-		
	-		O	DTR	7	8	RI	I	-		
	-	-	PWR	GND	9	10	5V	PWR	-	-	1

Note 1: The COM2 5V supply is fused with 1.1A resettable fuse.

Ribbon cable kits (Kontron PN 821016 or PN 821017) are available for converting the COM2 pin header connector to a DB9 connector for I/O panel.

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3.10 Ethernet Connectors

The KTG41 supports 2 channels of 10/100/1000Mb Ethernet via Marvell 88E8071 LAN controllers.

In order to achieve the specified performance of the Ethernet port, Category 5 twisted pair cables must be used with 10/100MB and Category 5E, 6 or 6E with 1Gb LAN networks.

The signals for the Ethernet ports are as follows:

Signal	Description
MDI[0]+ / MDI[0]-	In MDI mode, this is the first pair in 1000Base-T, i.e. the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
MDI[1]+ / MDI[1]-	In MDI mode, this is the second pair in 1000Base-T, i.e. the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
MDI[2]+ / MDI[2]-	In MDI mode, this is the third pair in 1000Base-T, i.e. the BI_DC+/- pair. In MDI crossover mode, this pair acts as the BI_DD+/- pair.
MDI[3]+ / MDI[3]-	In MDI mode, this is the fourth pair in 1000Base-T, i.e. the BI_DD+/- pair. In MDI crossover mode, this pair acts as the BI_DC+/- pair.

Note: MDI = Media Dependent Interface.

3.10.1 Ethernet Connectors 1 and 2 (ETHER1 and ETHER2)

Ethernet connector 1 is mounted together with USB Ports 4 and 5.
Ethernet connector 2 is mounted together with USB Ports 6 and 7.

The pinout of the RJ45 connectors is as follows:

Signal	PIN	Type	Ioh/Iol	Note
MDI0+				
MDI0-				
MDI1+				
MDI2+				
MDI2-				
MDI1-				
MDI3+				
MDI3-				
	8 7 6 5 4 3 2 1			

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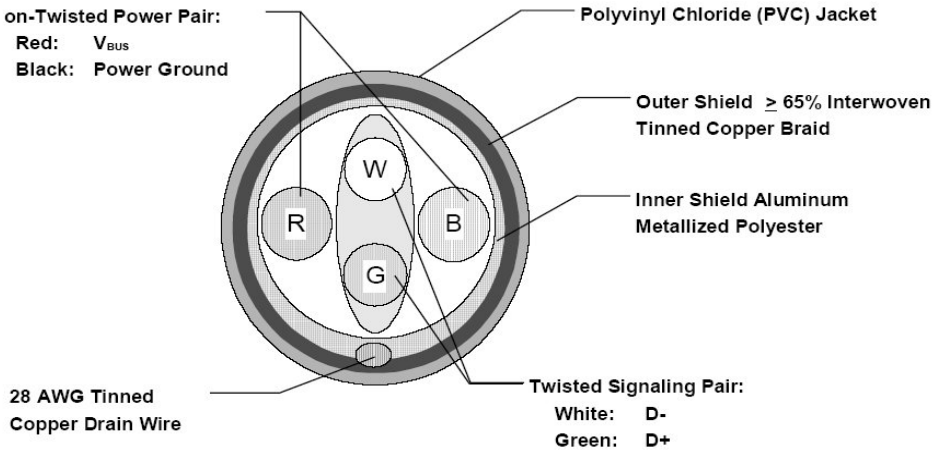
3.11 USB Connectors (USB)

The KTG41 contains two Enhanced Host Controller Interface (EHCI) host controllers that support USB 2.0 allowing data transfers up to 480Mb/s. The KTG41 also contains five Universal Host Controller Interface (UHCI Revision 1.1) controllers that support USB full-speed and low-speed signalling.
The KTG41 supports a total of eight USB 2.0 ports. All eight ports are high-speed, full-speed, and low-speed capable and USB Legacy mode is supported.

Over-current detection on all eight USB ports is supported.

USB Port 4 and 5 are supplied on the combined ETHER1, USB4, and USB5 connector.
USB Port 6 and 7 are supplied on the combined ETHER2, USB6, and USB7 connector.
USB Port 0 and 1 are supplied on the internal USB0/USB1 connector.
USB Ports 2 and 3 are supplied on the internal FRONTPNL connector; please refer to the FRONTPNL connector section for the pin-out.

Note: It is required to use only HiSpeed USB cable, specified in USB2.0 standard:



3.11.1 USB Connector 4/5 (USB4/5)

USB Ports 4 and 5 are mounted together with ETHER1 Ethernet port.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	-	-	PWR	5V/SB5V	1 2 3 4	GND	PWR	-	-	
	/15K	0.25/2	IO	USB5-		USB5+	IO	0.25/2	/15K	
1	-	-	PWR	5V/SB5V	1 2 3 4	GND	PWR	-	-	
	/15K	0.25/2	IO	USB4-		USB4+	IO	0.25/2	/15K	

Note 1: In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.

Signal	Description
USB4+ USB4- USB5+ USB5-	Differential pair works as Data/Address/Command Bus.
5V/SB5V	5V supply for external devices. SB5V is supplied during powerdown to allow wakeup on USB device activity. Protected by resettable 1.1A fuse covering both USB ports.

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3.11.2 USB Connector 6/7 (USB6/7)

USB Ports 6 and 7 are mounted together with ETHER2 Ethernet port.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	-	-	PWR	5V/SB5V	1 2 3 4	GND	PWR	-	-	
	/15K	0.25/2	IO	USB7-		USB7+	IO	0.25/2	/15K	
1	-	-	PWR	5V/SB5V	1 2 3 4	GND	PWR	-	-	
	/15K	0.25/2	IO	USB6-		USB6+	IO	0.25/2	/15K	

Note 1: In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.

Signal	Description
USB6+ USB6- USB7+ USB7-	Differential pair works as Data/Address/Command Bus.
5V/SB5V	5V supply for external devices. SB5V is supplied during powerdown to allow wakeup on USB device activity. Protected by resettable 1.1A fuse covering both USB ports.

3.11.3 USB Connector 0/1 (USB0/1)

USB Ports 0 and 1 are supplied on the internal USB0/USB1 pinrow connector.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1		-	PWR	5V/SB5V	1 2	5V/SB5V	PWR	-		1
		-	IO	USB0-	3 4	USB1-	IO		-	
	-		IO	USB0+	5 6	USB1+	IO	-		
	-		PWR	GND	7 8	GND	PWR	-		
	-	-		KEY	9 10	NC		-	-	

Note 1: In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.

Signal	Description
USB0+ USB0- USB1+ USB1-	Differential pair works as Data/Address/Command Bus.
5V/SB5V	5V supply for external devices. SB5V is supplied during powerdown to allow wakeup on USB device activity. Protected by resettable 1.1A fuse covering both USB ports.

3.11.4 USB Connector 2/3 (USB2/3)

See Frontpanel Connector (FRONTPNL) description.

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3.12 Audio Connectors

The onboard Audio circuit implements 7.1+2 Channel High Definition Audio with UAA (Universal Audio Architecture), featuring five 24-bit stereo DACs and three 20-bit stereo ADCs.

3.12.1 Audio Speakers, Line-In, Line-Out and Microphone

Audio Line-in, Line-out and Microphone are available in the stacked audiojack connector. Below is shown audio stack configuration when configured for 8-channel audio.

	Signal	Type	Note
TIP	LINE1-IN-L	IA	1
RING	LINE1-IN-R	IA	1
SLEEVE	GND	PWR	
TIP	FRONT-OUT-L	OA	
RING	FRONT-OUT-R	OA	
SLEEVE	GND	PWR	
TIP	MIC1-L	IA	1
RING	MIC1-R	IA	1
SLEEVE	GND	PWR	

Note 1: Signals are shorted to GND internally in the connector, when jack-plug not inserted.

Signal	Description	Note
FRONT-OUT-L	Front Speakers (Speaker Out Left).	
FRONT-OUT-R	Front Speakers (Speaker Out Right).	
MIC1	MIC Input 1	
LINE1-IN	Line in 1 signals	

Port	2-channel	4-channel	6-channel	8-channel
Light Blue	Line in	Line in	Line in	Line in
Lime	Line out	Front speaker out	Front speaker out	Front speaker out
Pink	Mic in	Mic in	Mic in	Mic in
Audio header	-	-	-	Side speaker out
Audio header	-	Rear speaker out	Rear speaker out	Rear speaker out
Audio header	-	-	Center/ Subwoofer	Center/ Subwoofer

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3.12.2 CDROM Audio Input (CDROM)

CD-ROM audio input may be connected to this connector. It may also be used as a secondary line-in signal.

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	CD_Left	IA	-	-	1
2	CD_GND	IA	-	-	
3	CD_GND	IA	-	-	
4	CD_Right	IA	-	-	1

Note 1: The definition of which pins are use for the Left and Right channels is not a worldwide accepted standard. Some CDROM cable kits expect reverse pin order.

Signal	Description
CD_Left CD_Right	Left and right CD audio input lines or secondary Line-in.
CD_GND	Analogue GND for Left and Right CD. (This analogue GND is **not** shorted to the general digital GND on the board).

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3.12.3 Audio Header (AUDIO_HEAD)

Note	Pull U/D	Ioh/ Iol	Type	Signal	PIN		Signal	Type	Ioh/ Iol	Pull U/D	Note
				LFE-OUT	1	2	CEN-OUT				
				AAGND	3	4	AAGND				
				FRONT-OUT-L	5	6	FRONT-OUT-R				
				AAGND	7	8	AAGND				
				REAR-OUT-L	9	10	REAR-OUT-R				
				SIDE-OUT-L	11	12	SIDE-OUT-R				
				AAGND	13	14	AAGND				
				MIC1-L	15	16	MIC1-R				
				AAGND	17	18	AAGND				
				LINE1-IN-L	19	20	LINE1-IN-R				
				NC	21	22	AAGND				
	-	-	PWR	GND	23	24	SPDIF-IN				
				SPDIF-OUT	25	26	GND	PWR	-	-	

Signal	Description	Note
FRONT-OUT-L	Front Speakers (Speaker Out Left).	
FRONT-OUT-R	Front Speakers (Speaker Out Right).	
REAR-OUT-L	Rear Speakers (Surround Out Left).	
REAR-OUT-R	Rear Speakers (Surround Out Right).	
SIDE-OUT-L	Side speakers (Surround Out Left)	
SIDE-OUT-R	Side speakers (Surround Out Right)	
CEN-OUT	Center Speaker (Center Out channel).	
LFE-OUT	Subwoofer Speaker (Low Freq. Effect Out).	
NC	No connection	
MIC1	MIC Input 1	
LINE1-IN	Line in 1 signals	
F-SPDIF-IN	S/PDIF Input	
F-SPDIF-OUT	S/PDIF Output	
AAGND	Audio Analogue ground	

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3.13 Fan Connector (FAN_CPU)

The **FAN_CPU** is used for the connection of the FAN for the CPU.
The **FAN_SYS** can be used to power, control and monitor a fan for chassis ventilation etc.

The 4pin header supports connection of 3-pin FAN, but it is recommended to use the 4-pin type for optimized FAN speed control. The 3- or 4-pin mode is set in the BIOS setup menu.

4-pin Mode:

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	CONTROL	O	-	-	
2	SENSE	I	-	4K7	
3	+12V	PWR	-	-	
4	GND	PWR	-	-	

Signal	Description
CONTROL	PWM signal for FAN speed control
SENSE	Tacho signal from the fan for supervision. The signals shall be generated by an open collector transistor or similar. Onboard is a pull-up resistor 4K7 to +12V. The signal has to be pulsed, typically twice per rotation.
12V	+12V supply for fan. A maximum of 2000mA can be supplied from this pin.
GND	Power Supply GND signal

3-pin Mode:

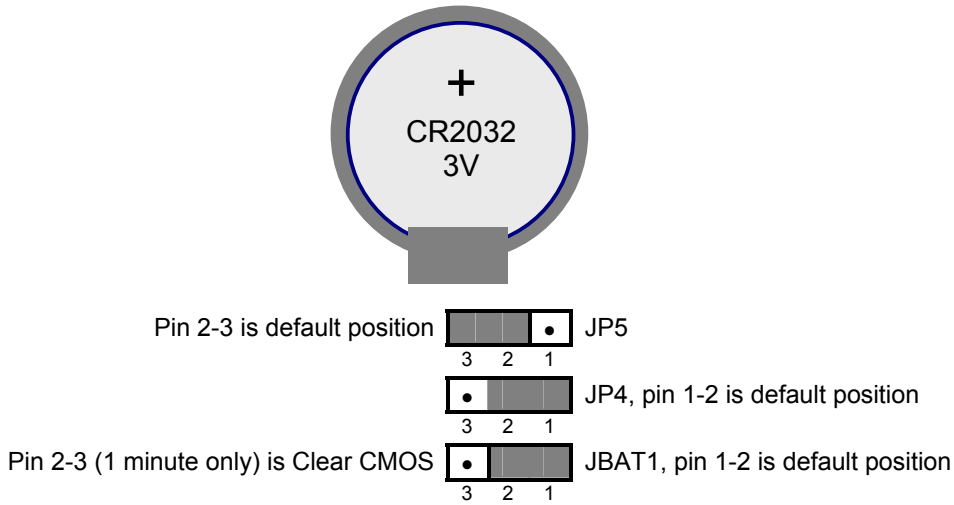
PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
-					
2	SENSE	I	-	4K7	
3	+12V	PWR	-	-	
4	GND	PWR	-	-	

Signal	Description
SENSE	Tacho signal from the fan for supervision. The signals shall be generated by an open collector transistor or similar. Onboard is a pull-up resistor 4K7 to +12V. The signal has to be pulsed, typically twice per rotation.
12V	+12V supply for fan, can be turned on/off or modulated (PWM) by the chipset. A maximum of 2000mA can be supplied from this pin.
GND	Power Supply GND signal

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3.14 Clear CMOS Jumper (Clr-CMOS /JBAT1)

The Clr-CMOS Jumper is used to clear the CMOS content.



To clear all CMOS settings, including Password protection, move the Clr-CMOS jumper to pin 2-3 for 1 minute (Works with or without power connected to the system).

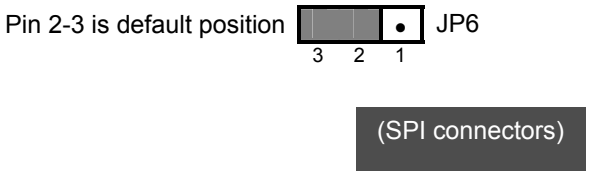
WARNING: Don't leave the jumper in Clear CMOS position, otherwise without power connected to the system the battery will fully depleted within a few weeks.

WARNING: JP4 and JP5 are used to select the BIOS to boot. These jumpers are for manufacturing purpose only and they shall always be in the positions indicated above (JP4 Jumper in position 1-2 and JP5 Jumper in position 2-3). If one or both Jumpers are not in correct position the KTG41 will not boot BIOS.

3.15 The SPI Jumper (SPI-Jumper / JP6)

The SPI selection jumper is used to switch between onboard SPI and external SPI device.

Note: The SPI device holds the BIOS contents and should not be removed from its default position unless a pre-programmed SPI device is connected to the SPI1 connector.



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3.16 TPM Connector (TPM)

This connector is unsupported.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	LPC CLK	1	2	GND				
	-	-	PWR	LPC FRAME#	3		KEY				
				LPC RST#	5	6	+5V				
				LPC AD3	7	8	LPC AD2				
				+3V3	9	10	LPC AD1				
				LPC AD0	11	12	GND				
				SMB_CLK	13	14	SMB_DATA				
				SB3V3	15	16	LPC SERIRQ				
				GND	17	18	CLKRUN#				
				SUS_STAT#	19	20	NC				

3.17 SPI Connector (SPI)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
				SPI_CLK	1	2	SB3V3	PWR	-	-	
	-	-	-	NC	3	4	BOOT0	IO		-	
	10K/			SPI_CS2#	5	6	BOOT1	IO	-		
	10K/			SPI_MOSI	7	8	MFG		-		
	10K/			SPI_MISO	9	10	GND	PWR	-	-	

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3.18 Front Panel Connector (FRONTPNL)

Note	Pull U/D	Ioh/ Iol	Type	Signal	PIN		Signal	Type	Ioh/ Iol	Pull U/D	Note
				USB10/11_5V	1	2	USB10/11_5V				
				USB1-	3	4	USB3-				
				USB1+	5	6	USB3+				
	-	-	PWR	GND	7	8	GND	PWR	-	-	
	-	-	-	NC	9	10	LINE2-IN-L	-	-	-	
	-	-	PWR	+5V	11	12	+5V	PWR	-	-	
			OC	HD_LED	13	14	SUS_LED				
	-	-	PWR	GND	15	16	PWRBTN_IN#				
				RSTIN#	17	18	GND	PWR	-	-	
				SB3V3	19	20	LINE2-IN-R	-	-	-	
				AGND	21	22	AGND				
				MIC2-L	23	24	MIC2-R				

Signal	Description
USB10/11_5V	5V supply for external devices. SB5V is supplied during powerdown to allow wakeup on USB device activity. Protected by resettable 1.1A fuse covering both USB ports.
USB1+ USB1-	Universal Serial Bus Port 1 Differentials: Bus Data/Address/Command Bus.
USB3+ USB3-	Universal Serial Bus Port 3 Differentials: Bus Data/Address/Command Bus.
+5V	Maximum load is 1A or 2A per pin if using IDC connector flat cable or crimp terminals respectively.
HD_LED	Hard Disk Activity LED (active low signal). Output is via 475Ω to OC.
SUS_LED	Suspend Mode LED (active high signal). Output is via 475Ω.
PWRBTN_IN#	Power Button In. Toggle this signal low to start the ATX / BTX PSU and boot the board.
RSTIN#	Reset Input. When pulled low for a minimum 16ms, the reset process will be initiated. The reset process continues even though the Reset Input is kept low.
LINE2-IN	Line in 2 signals
MIC2	MIC2-L and MIC2-R is second stereo microphone input.
SB3V3	Standby 3.3V voltage
AGND	Analogue Ground for Audio

Note 1: In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.

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3.19 Feature Connector (FEATURE)

Note	Pull U/D	Ioh/ Iol	Type	Signal	PIN		Signal	Type	Ioh/ Iol	Pull U/D	Note
2	243K/	-	I	INTRUDER#	1	2	GND	PWR	-	-	
				EXT_ISAIRQ#	3	4	EXT_SMI#	I		2K7	3
				PWR_OK	5	6	SB5V	PWR	-	-	
	-	-	PWR	SB3V3	7	8	EXT_BAT	PWR	-	-	
	-	-	PWR	+5V	9	10	GND	PWR	-	-	
1	2K7/	/12mA	IOT	GPIO0	11	12	GPIO1	IOT	/12mA	2K7/	1
1	2K7/	/12mA	IOT	GPIO2	13	14	GPIO3	IOT	/12mA	2K7/	1
1	2K7/	/12mA	IOT	GPIO4	15	16	GPIO5	IOT	/12mA	2K7/	1
1	2K7/	/12mA	IOT	GPIO6	17	18	GPIO7	IOT	/12mA	2K7/	1
	-	-	PWR	GND	19	20	FAN3OUT	O		2K7	3
				FAN3IN	21	22	+12V	PWR	-	-	
				TEMP3IN	23	24	VREF				
	-	-	PWR	GND	25	26	IRRX				
				IRTX	27	28	GND	PWR	-	-	
1	2K7/			SMBC	29	30	SMBD			2K7/	1

Notes:

1. Pull-up to +3V3Dual (+3V3 or SB3V3).
2. Pull-up to +3V3Dual and power backup by onboard Battery.
3. Pull-up to +3V3.

Signal	Description
INTRUDER#	INTRUDER, may be used to detect if the system case has been opened. This signal's status is readable, so it may be used like a GPI when the Intruder switch is not required.
EXT_ISAIRQ#	EXTernal ISA IRQ, (active low input) can activate standard AT-Bus IRQ-interrupt.
EXT_SMI#	External SMI, (active low input) signal can activate SMI interrupt.
PWR_OK	PoWeR OK, signal is high if no power failures are detected.
SB5V	StandBy +5V supply.
SB3V3	Max. load is 0.75A (1.5A < 1 sec.)
EXT_BAT	(EXTernal BATtery) option for connecting + terminal of an external primary cell battery (2.5 - 4.0 V) (– terminal connected to GND etc. pin 10). The external battery is protected against charging and can be used with or without the onboard battery installed.
+5V	Max. load is 0.75A (1.5A < 1 sec.)
GPIO0..7	General Purpose Inputs / Output. These Signals may be controlled or monitored through the use of the KT-API-V2 (Application Programming Interface).
FAN3OUT	FAN 3 speed control OUTput. This 3.3V PWM signal can be used as Fan control voltage (0–3.3V DC in 128 steps) via a Fan Driver Circuit (not included) to program Fan voltage. For more info, see W83627 datasheet. Default PMW output is 127 (100% = 3.3V).
FAN3IN	FAN3 Input. 0V to +3V3 amplitude Fan 3 tachometer input.
+12V	Max. load is 0.75A (1.5A < 1 sec.)
TEMP3IN	Temperature sensor 3 input. (Recommended: Transistor 2N3904, having emitter connected to GND (pin 25), collector and basis shorted and connected to pin 23. Further a resistor 30K/1% shall be connected between pin 23 - 24. (Precision +/- 3ºC).
VREF	Voltage REFerence, reference voltage to be used with TEMP3IN input.
IRRX	IR Receive input (IrDA 1.0, SIR up to 1.152K bps)
IRTX	IR Transmit output (IrDA 1.0, SIR up to 1.152K bps)
SMBC	SMBus Clock signal
SMBD	SMBus Data signal

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3.20 PCI Slot Connector (PCI Slot)

Note	Type	Signal	Terminal S	Terminal C	Signal	Type	Note
	PWR	-12V	F01	E01	TRST#	O	
	O	TCK	F02	E02	+12V	PWR	
	PWR	GND	F03	E03	TMS	O	
	I	TDO	F04	E04	TDI	O	
	PWR	+5V	F05	E05	+5V	PWR	
	PWR	+5V	F06	E06	INTA#	I	
	I	INTB#	F07	E07	INTC#	I	
	I	INTD#	F08	E08	+5V	PWR	
	I	REQ2#	F09	E09	CLKC	O	
	I	REQ3#	F10	E10	+5V (I/O)	PWR	
	OT	GNT2#	F11	E11	CLKD	O	
	PWR	GND	F12	E12	GND	PWR	
	PWR	GND	F13	E13	GND	PWR	
	O	CLKA	F14	E14	GNT3#	OT	
	PWR	GND	F15	E15	RST#	O	
	O	CLKB	F16	E16	+5V (I/O)	PWR	
	PWR	GND	F17	E17	GNT0#	OT	
	I	REQ0#	F18	E18	GND	PWR	
	PWR	+5V (I/O)	F19	E19	REQ1#	I	
	IOT	AD31	F20	E20	AD30	IOT	
	IOT	AD29	F21	E21	+3.3V	PWR	
	PWR	GND	F22	E22	AD28	IOT	
	IOT	AD27	F23	E23	AD26	IOT	
	IOT	AD25	F24	E24	GND	PWR	
	PWR	+3.3V	F25	E25	AD24	IOT	
	IOT	C/BE3#	F26	E26	GNT1#	OT	
	IOT	AD23	F27	E27	+3.3V	PWR	
	PWR	GND	F28	E28	AD22	IOT	
	IOT	AD21	F29	E29	AD20	IOT	
	IOT	AD19	F30	E30	GND	PWR	
	PWR	+3.3V	F31	E31	AD18	IOT	
	IOT	AD17	F32	E32	AD16	IOT	
	IOT	C/BE2#	F33	E33	+3.3V	PWR	
	PWR	GND	F34	E34	FRAME#	IOT	
	IOT	IRDY#	F35	E35	GND	PWR	
	PWR	+3.3V	F36	E36	TRDY#	IOT	
	IOT	DEVSEL#	F37	E37	GND	PWR	
	PWR	GND	F38	E38	STOP#	IOT	
	IOT	LOCK#	F39	E39	+3.3V	PWR	
	IOT	PERR#	F40	E40	SDONE	IO	
	PWR	+3.3V	F41	E41	SB0#	IO	
	IOC	SERR#	F42	E42	GND	PWR	
	PWR	+3.3V	F43	E43	PAR	IOT	
	IOT	C/BE1#	F44	E44	AD15	IOT	
	IOT	AD14	F45	E45	+3.3V	PWR	
	PWR	GND	F46	E46	AD13	IOT	
	IOT	AD12	F47	E47	AD11	IOT	
	IOT	AD10	F48	E48	GND	PWR	
	PWR	GND	F49	E49	AD09	IOT	
SOLDER SIDE					COMPONENT SIDE		
	IOT	AD08	F52	E52	C/BE0#	IOT	
	IOT	AD07	F53	E53	+3.3V	PWR	
	PWR	+3.3V	F54	E54	AD06	IOT	
	IOT	AD05	F55	E55	AD04	IOT	
	IOT	AD03	F56	F56	GND	PWR	
	PWR	GND	F57	E57	AD02	IOT	
	IOT	AD01	F58	E58	AD00	IOT	
	PWR	+5V (I/O)	F59	E59	+5V (I/O)	PWR	
	IOT	ACK64#	F60	E60	REQ64#	IOT	
	PWR	+5V	F61	E61	+5V	PWR	
	PWR	+5V	F62	E62	+5V	PWR	

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3.20.1 Signal Description – PCI Slot Connector

SYSTEM PINS	
CLK	Clock provides timing for all transactions on PCI and is an input to every PCI device. All other PCI signals, except RST#, INTA#, INTB#, INTC#, and INTD#, are sampled on the risingedge of CLK and all other timing parameters are defined with respect to this edge. PCI operates at 33MHz.
RST#	Reset is used to bring PCI-specific registers, sequencers, and signals to a consistent state. What effect RST# has on a device beyond the PCI sequencer is beyond the scope of this specification, except for reset states of required PCI configuration registers. Anytime RST# is asserted, all PCI output signals must be driven to their benign state. In general, this means they must be asynchronously tri-stated. SERR# (open drain) is floated. REQ# and GNT# must both be tri-stated (they cannot be driven low or high during reset). To prevent AD, C/BE#, and PAR signals from floating during reset, the central resource may drive these lines during reset (bus parking) but only to a logic low level–they may not be driven high. RST# may be asynchronous to CLK when asserted or deasserted. Although asynchronous, deassertion is guaranteed to be a clean, bounce-free edge. Except for configuration accesses, only devices that are required to boot the system will respond after reset.
ADDRESS AND DATA	
AD[31::00]	Address and Data are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. PCI supports both read and write bursts. The address phase is the clock cycle in which FRAME# is asserted. During the address phase AD[31::00] contain a physical address (32 bits). For I/O, this is a byte address; for configuration and memory, it is a DWORD address. During data phases AD[07::00] contain the least significant byte (lsb) and AD[31::24] contain the most significant byte (msb). Write data is stable and valid when IRDY# is asserted and read data is stable and valid when TRDY# is asserted. Data is transferred during those clocks where both IRDY# and TRDY# are asserted.
C/BE[3::0]#	Bus Command and Byte Enables are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3::0]# define the bus command. During the data phase C/BE[3::0]# are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. C/BE[0]# applies to byte 0 (lsb) and C/BE[3]# applies to byte 3 (msb).
PAR	Parity is even parity across AD[31::00] and C/BE[3::0]#. Parity generation is required by all PCI agents. PAR is stable and valid one clock after the address phase. For data phases, PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase. (PAR has the same timing as AD[31::00], but it is delayed by one clock.) The master drives PAR for address and write data phases; the target drives PAR for read data phases.
INTERFACE CONTROL PINS	
FRAME#	Cycle Frame is driven by the current master to indicate the beginning and duration of an access. FRAME# is asserted to indicate a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is deasserted, the transaction is in the final data phase or has completed.
IRDY#	Initiator Ready indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. A data phase is completed on any clock both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates that valid data is present on AD[31::00]. During a read, it indicates the master is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.
TRDY#	Target Ready indicates the target agent's (selected device's) ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed on any clock both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that valid data is present on AD[31::00]. During a write, it indicates the target is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.
STOP#	Stop indicates the current target is requesting the master to stop the current transaction.
LOCK#	Lock indicates an atomic operation that may require multiple transactions to complete. When LOCK# is asserted, non-exclusive transactions may proceed to an address that is not currently locked. A grant to start a transaction on PCI does not guarantee control of LOCK#. Control of LOCK# is obtained under its own protocol in conjunction with GNT#. It is possible for different agents to use PCI while a single master retains ownership of LOCK#. If a device implements Executable Memory, it should also implement LOCK# and guarantee complete access exclusion in that memory. A target of an access that supports LOCK# must provide exclusion to a minimum of 16 bytes (aligned). Host bridges that have system memory behind them should implement LOCK# as a target from the PCI bus point of view and optionally as a master.
IDSEL	Initialization Device Select is used as a chip select during configuration read and write transactions.
DEVSEL#	Device Select, when actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.

(Continues)

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ARBITRATION PINS (BUS MASTERS ONLY)	
REQ#	Request indicates to the arbiter that this agent desires use of the bus. This is a point to point signal. Every master has its own REQ# which must be tri-stated while RST# is asserted.
GNT#	Grant indicates to the agent that access to the bus has been granted. This is a point to point signal. Every master has its own GNT# which must be ignored while RST# is asserted. While RST# is asserted, the arbiter must ignore all REQ# lines since they are tri-stated and do not contain a valid request. The arbiter can only perform arbitration after RST# is deasserted. A master must ignore its GNT# while RST# is asserted. REQ# and GNT# are tri-state signals due to power sequencing requirements when 3.3V or 5.0V only add-in boards are used with add-in boards that use a universal I/O buffer.
ERROR REPORTING PINS. The error reporting pins are required by all devices and maybe asserted when enabled	
PERR#	Parity Error is only for the reporting of data parity errors during all PCI transactions except a Special Cycle. The PERR# pin is sustained tri-state and must be driven active by the agent receiving data two clocks following the data when a data parity error is detected. The minimum duration of PERR# is one clock for each data phase that a data parity error is detected. (If sequential data phases each have a data parity error, the PERR# signal will be asserted for more than a single clock.) PERR# must be driven high for one clock before being tri-stated as with all sustained tri-state signals. There are no special conditions when a data parity error may be lost or when reporting of an error may be delayed. An agent cannot report a PERR# until it has claimed the access by asserting DEVSEL# (for a target) and completed a data phase or is the master of the current transaction.
SERR#	System Error is for reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic. If an agent does not want a non-maskable interrupt (NMI) to be generated, a different reporting mechanism is required. SERR# is pure open drain and is actively driven for a single PCI clock by the agent reporting the error. The assertion of SERR# is synchronous to the clock and meets the setup and hold times of all bused signals. However, the restoring of SERR# to the deasserted state is accomplished by a weak pullup (same value as used for s/t/s) which is provided by the system designer and not by the signaling agent or central resource. This pull-up may take two to three clock periods to fully restore SERR#. The agent that reports SERR#s to the operating system does so anytime SERR# is sampled asserted.
INTERRUPT PINS (OPTIONAL). Interrupts on PCI are optional and defined as “level sensitive,” asserted low (negative true), using open drain output drivers. The assertion and deassertion of INTx# is asynchronous to CLK. A device asserts its INTx# line when requesting attention from its device driver. Once the INTx# signal is asserted, it remains asserted until the device driver clears the pending request. When the request is cleared, the device deasserts its INTx# signal. PCI defines one interrupt line for a single function device and up to four interrupt lines for a multi-function device or connector. For a single function device, only INTA# may be used while the other three interrupt lines have no meaning.	
INTA#	Interrupt A is used to request an interrupt.
INTB#	Interrupt B is used to request an interrupt and only has meaning on a multi-function device.
INTC#	Interrupt C is used to request an interrupt and only has meaning on a multi-function device.
INTD#	Interrupt D is used to request an interrupt and only has meaning on a multi-function device.

3.20.2 KTG41 PCI IRQ & INT routing

Board type	Slot	IDSEL	INTA	INTB	INTC	INTD
KTG41/ATXu	1	AD16	INT_PIRQ#A	INT_PIRQ#B	INT_PIRQ#C	INT_PIRQ#D
	2	AD17	INT_PIRQ#E	INT_PIRQ#F	INT_PIRQ#G	INT_PIRQ#H

When using the 820982 “PCI Riser - Flex - 2slot w. arbiter” the lower slot has IDSEL / IRQs routed straight through and the top slot has the routing: IDSEL=AD22, INT_PIRQ#F, INT_PIRQ#G, INT_PIRQ#H, INT_PIRQ#E. 820982 PCI Riser shall be plugged into Slot #1.

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4 Onboard connectors and Mating connectors

Connector	Onboard Connectors		Mating Connectors	
	Manufacturer	Type no.	Manufacturer	Type no.
FAN_CPU	Foxconn	HF2704E-M1	AMP	1375820-4 (4-pole)
FAN_SYS	AMP	1470947-1	AMP	1375820-3 (3-pole)
KBDMSE	Molex	22-23-2061	Molex	22-01-2065
CDROM	Foxconn	HF1104E	Molex	50-57-9404
	Molex	70543-0038		
SATA1-4	Hon Hai	LD1807V-S52T	Molex	67489-8005
			Kontron	KT 821035 (cable kit)
ATXPWR	Molex	43045-1201	Molex	43025-1200
			Kontron	KT 1022-6309 (cable kit for ATX PSU)
ATX+12V-4pin	Molex	22-23-2041	Molex	22-01-2046
			Kontron	KT 1027-3669 (cable kit)
ATX+12V-6pin	Molex	22-23-2041	Molex	22-01-2046
			Kontron	KT 1027-3669 (cable kit)
COM2	Wuerth	61201020621	Molex	90635-1103
			Kontron	KT 821016 (cable kit)
			Kontron	KT 821017 (cable kit)
USB0/USB1	Pinrex	512-90-10GBB2	Kontron	KT 821401 (cable kit)
USB2/USB3*	(FRONTPNL)	-	Kontron	KT 821401 (cable kit)
PRINTER	Foxconn	HL2213F	Molex	90635-1263
			Kontron	KT 821031 (cable kit)
AUDIO_HEAD	Molex	87831-2620	Molex	51110-2651
			Kontron	KT 821043 (cable kit)
FRONTPNL	Pinrex	512-90-24GBB3	Molex	90635-1243
			Kontron	KT 821042 (cable kit)
FEATURE	Molex	87831-3020	Molex	51110-3051
			Kontron	KT 821041 (cable kit)

* USB2/USB3 is located in FRONTPNL connector. Depending on application the KT821401 can be used.

Note: Only one connector will be mentioned for each type of onboard connector even though several types with same fit, form and function are approved and could be used as alternative. Please also notice that standard connectors like DVI, PCIe, PCI, CF, Ethernet and USB is not included in the list.

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5 System Resources

5.1 Memory Map

Address (hex)		Size	Description
00000000	0009FFFF	655360	System board
000A0000	000BFFFF	131072	PCI-bus
000A0000	000BFFFF	131072	Intel(R) G41 Express Chipset
000C0000	000CFFFF	65536	System board
000D0000	000DFFFF	65536	PCI-bus
000E0000	000FFFFF	131072	System board
00100000	3DDFFFFF	1037041664	System board
3DE00000	DFFFFFFF	2720006144	PCI-bus
D0000000	DFFFFFFF	268435456	Intel(R) G41 Express Chipset
E0000000	EFFFFFFF	268435456	Motherboard resources
F0000000	FFFFFFFF	268435456	PCI-bus
FE400000	FE7FFFFF	4194304	Intel(R) G41 Express Chipset
FE9F8000	FE9FBFFF	16384	Microsoft UAA-bus driver for High Definition Audio
FE9FF800	FE9FFBFF	1024	Intel(R) 82801GB (ICH7) USB2 Enhanced Host Controller
FE9FFC00	FE9FFFFF	1024	Intel(R) 82801GB (ICH7) Serial ATA Storage Controller
FEA00000	FEAFFFFF	1048576	Intel(R) 82801GB (ICH7) PCI Express Root Port
FEAFC000	FEAFFFFF	16384	Marvell Yukon 88E8071 PCI-E Gigabit Ethernet Controller
FEB00000	FEBFFFFF	1048576	Intel(R) 82801GB (ICH7) PCI Express Root Port
FEBFC000	FEBFFFFF	16384	Marvell Yukon 88E8071 PCI-E Gigabit Ethernet Controller #2
FEC00000	FEC00FFF	4096	Motherboard resources
FED14000	FED19FFF	24576	System board
FED1C000	FED1FFFF	16384	Motherboard resources
FED20000	FED3FFFF	131072	Motherboard resources
FED90000	FED93FFF	16384	System board
FEE00000	FEE00FFF	4096	Motherboard resources
FFB00000	FFBFFFFF	1048576	Intel(R) 82802 Firmware Hub
FFC00000	FFEFFFFF	3145728	Motherboard resources
FFF00000	FFFFFFFF	1048576	Intel(R) 82802 Firmware Hub

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5.2 PCI Devices

Bus #	Device #	Function #	Vendor ID	Device ID	Chip	Device Function
0	0	0	8086	2E30	Intel G41	Host bridge
0	2	0	8086	2E32	Intel G41	VGA Controller
0	27	0	8086	27D8	Intel ICH7	High Definition Audio
0	28	0	8086	27D0	Intel ICH7	PCI to PCI bridge
0	28	4	8086	27E0	Intel ICH7	PCI to PCI bridge
0	28	5	8086	27E2	Intel ICH7	PCI to PCI bridge
0	29	0	8086	27C8	Intel ICH7	USB Universal Host Controller
0	29	1	8086	27C9	Intel ICH7	USB Universal Host Controller
0	29	2	8086	27CA	Intel ICH7	USB Universal Host Controller
0	29	3	8086	27CB	Intel ICH7	USB Universal Host Controller
0	29	7	8086	27CC	Intel ICH7	USB Universal Host Controller
0	30	0	8086	244E	Intel ICH7 I/O	PCI to PCI bridge
0	31	0	8086	27B8	Intel ICH7	ISA bridge
0	31	1	8086	27DF	Intel ICH7	IDE Controller
0	31	2	8086	27C0	Intel ICH7	IDE Controller
0	31	3	8086	27DA	Intel ICH7	SMBus
2	0	0	11AB	436B	Marvell 88E8071	Ethernet Controller
3	0	0	11AB	436B	Marvell 88E8071	Ethernet Controller

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5.3 Interrupt Usage

IRQ	System timer	Keyboard	Communications port COM1 Selection in BIOS	Communications port COM2 Selection in BIOS	Intel(R) ICH7 SMBus Controller	Parallel port Selection in BIOS	System CMOS/real-time watch	Microsoft ACPI-compatible system	Microsoft PS/2-mus	Numerical Data Processor	Primary IDE-channel	Secondary IDE-channel	Marvell Yukon 88E8071 Gigabit Ethernet Controller #2	Intel(R) 82801G ICH7 USB Universal Host Controller	Intel(R) 82801G ICH7 PCI Express Root Port	Intel(R) 82801GR/GH/GHM ICH7 PCI Express Root Port	Microsoft UAA-bus driver for High Definition Audio	Intel(R) G41 Express Chipset	Marvell Yukon 88E8071 Gigabit Ethernet Controller	Intel(R) 82801GR/GH/GHM ICH7 PCI Express Root Port	Intel(R) 82801G ICH7 USB Universal Host Controller	Intel(R) 82801GB/GR/GH (ICH7 Family) Serial ATA Storage	Intel(R) 82801G (ICH7 Family) USB2 Enhanced Host Controller
NMI																							
IRQ0	X																						
IRQ1		X																					
IRQ2																							
IRQ3				X																			
IRQ4			X																				
IRQ5					X																		
IRQ6																							
IRQ7						X																	
IRQ8							X																
IRQ9								X															
IRQ10																							
IRQ11																							
IRQ12									X														
IRQ13										X													
IRQ14											X												
IRQ15												X											
IRQ16													X	X	X	X	X	X					
IRQ17																			X	X			
IRQ18																					X		
IRQ19																					X	X	
IRQ20																							
IRQ21																							
IRQ22																							
IRQ23																					X		X
IRQ24																							
IRQ25																							
IRQ26																							

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5.4 IO Map

Address range (hex)		Size	Description
0	0F	16	DMA-controller
0	0CF7	3320	PCI-bus
10	1F	16	Motherboard resources
20	21	2	Programmable interrupt controller
22	2D	30	Motherboard resources
30	3F	16	Motherboard resources
40	43	4	System timer
44	5F	28	Motherboard resources
60	60	1	Standard keyboard
61	61	1	System Speaker
62	63	2	Motherboard resources
64	64	1	Standard keyboard
65	6F	11	Motherboard resources
70	71	2	System CMOS/Real time clock
72	7F	14	Motherboard resources
80	80	1	Motherboard resources
81	83	3	DMA-controller
84	86	3	Motherboard resources
87	87	1	DMA-controller
88	88	1	Motherboard resources
89	8B	3	DMA-controller
8C	8E	3	Motherboard resources
8F	8F	1	DMA-controller
90	9F	16	Motherboard resources
A0	A1	2	Programmable interrupt controller
A2	BF	30	Motherboard resources
C0	DF	32	DMA-controller
E0	EF	16	Motherboard resources
F0	FF	16	Numerical Data Processor
170	177	8	Secondary IDE-channel
01F0	01F7	8	Primary IDE-channel
274	277	4	ISAPNP read data port
279	279	1	ISAPNP read data port
02F8	02FF	8	Communications port (COM2)
376	376	1	Secondary IDE-channel
378	037F	8	Printer Port (LPT1)
03B0	03BB	12	Intel(R) G41 Express Chipset
03C0	03DF	32	Intel(R) G41 Express Chipset
03F6	03F6	1	Primary IDE-channel
03F8	03FF	8	Communications port (COM1)
400	041F	32	Intel(R) 82801G (ICH7 Family) SMBus Controller - 27DA
480	4BF	64	Motherboard resources
04D0	04D1	2	Motherboard resources
500	057F	128	Motherboard resources
800	087F	128	Motherboard resources
0A00	0A0F	16	Motherboard resources
0A10	0A1F	16	Motherboard resources
0A79	0A79	1	ISAPNP read data port
0D00	FFFF	62208	PCI-bus
B800	B807	8	Intel(R) G41 Express Chipset
B880	B89F	32	Intel(R) 82801G (ICH7 Family) USB Universal Host Controller - 27C8
BC00	BC0F	16	Intel(R) 82801G (ICH7 Family) USB Universal Host Controller - 27C9
C000	C01F	32	Intel(R) 82801G (ICH7 Family) USB Universal Host Controller - 27CA
C080	C09F	32	Intel(R) 82801G (ICH7 Family) USB Universal Host Controller - 27CB
C400	C40F	16	Intel(R) 82801GB/GR/GH (ICH7 Family) Serial ATA Storage Controller - 27C0
C480	C483	4	Intel(R) 82801GB/GR/GH (ICH7 Family) Serial ATA Storage Controller - 27C0
C800	C803	4	Intel(R) 82801GB/GR/GH (ICH7 Family) Serial ATA Storage Controller - 27C0
C880	C883	4	Intel(R) 82801GB/GR/GH (ICH7 Family) Serial ATA Storage Controller - 27C0
CC00	CC07	8	Intel(R) 82801GB/GR/GH (ICH7 Family) Serial ATA Storage Controller - 27C0
D000	DFFF	4096	Intel(R) 82801GR/GH/GHM (ICH7 Family) PCI Express Root Port - 27E2
D800	D8FF	265	Marvell Yukon 88E8071 PCI-E Gigabit Ethernet Controller
E000	EFFF	4096	Intel(R) 82801GR/GH/GHM (ICH7 Family) PCI Express Root Port - 27E0
E800	E8FF	265	Marvell Yukon 88E8071 PCI-E Gigabit Ethernet Controller #2
FFA0	FFAF	16	Intel(R) 82801G (ICH7 Family) Ultra ATA Storage Controllers - 27DF

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6 Overview of BIOS Features

This section details specific BIOS features for the KTG41 board.
The KTG41 is based on the AMI BIOS core version 8.00 with Kontron BIOS extensions.

6.1 System Management BIOS (SMBIOS/DMI)

SMBIOS is a Desktop Management Interface (DMI) compliant method for managing computers in a managed network.

The main component of SMBIOS is the Management Information Format (MIF) database, which contains information about the computing system and its components. Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components.

The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as third-party management software to use SMBIOS.

The BIOS stores and reports the following SMBIOS information:
• BIOS data, such as the BIOS revision level
• Fixed-system data, such as peripherals, serial numbers, and asset tags
• Resource data, such as memory size, cache size, and processor speed
• Dynamic data, such as event detection and error logging

Non-Plug and Play operating systems, such as Windows NT*, require an additional interface for obtaining the SMBIOS information. The BIOS supports an SMBIOS table interface for such operating systems. Using this support, an SMBIOS service-level application running on a non-Plug and Play operating system can obtain the SMBIOS information.

6.2 Legacy USB Support

Legacy USB support enables USB devices such as keyboards, mice, and hubs to be used even when the operating system's USB drivers are not yet available. Legacy USB support is used to access the BIOS Setup program, and to install an operating system that supports USB. By default, Legacy USB support is Enabled.

Legacy USB support operates as follows:

1. When you apply power to the computer, legacy support is disabled.
2. POST begins.
3. Legacy USB support is enabled by the BIOS allowing you to use a USB keyboard to enter and configure the BIOS Setup program and the maintenance menu.
4. POST completes.
5. The operating system loads. While the operating system is loading, USB keyboards and mice are recognized and may be used to configure the operating system. (Keyboards and mice are not recognized during this period if Legacy USB support is Disabled in the BIOS Setup.)
6. After the operating system loads the USB drivers, all legacy and non-legacy USB devices are recognized by the operating system, and Legacy USB support from the BIOS is no longer used.

To install an operating system that supports USB, verify that Legacy USB support in the BIOS Setup program is set to Enabled and follow the operating system's installation instructions.

6.3 BIOS Update

The BIOS can be updated using Kontron utility called bf.exe, which are included in BIOS packages available on the Kontron Web site. The utility supports DOS and Windows environment.

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BIOS Configuration/Setup

6.4 Introduction

The BIOS Setup is used to view and configure BIOS settings for the KTG41 board. The BIOS Setup is accessed by pressing the DEL key after the Power-On Self-Test (POST) memory test begins and before the operating system boot begins. The Menu bar looks like this:

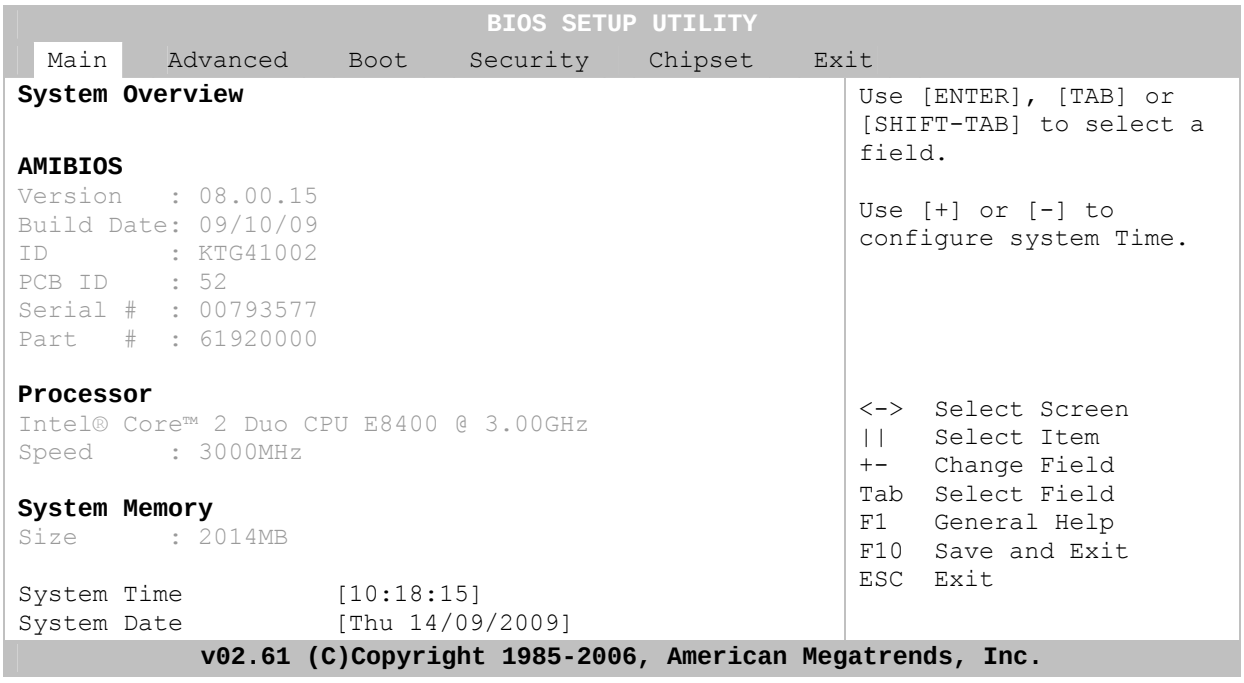


The available keys for the Menu screens are:

Select Menu: <←> or <→>
Select Item: <↑> or <↓>
Select Field: <Tab>
Change Field: <+> or <->
Help: <F1>
Save and Exit: <F10>
Exits the Menu: <Esc>

Please note that in the following the different BIOS Features will be described as having some options. These options will be selected automatically when loading either Failsafe Defaults or Optimal Defaults. The Default options will be indicated by the option in **bold**, but please notice that when Failsafe Defaults are loaded a few of the options, marked with "*", are now the default option.

6.5 Main Menu

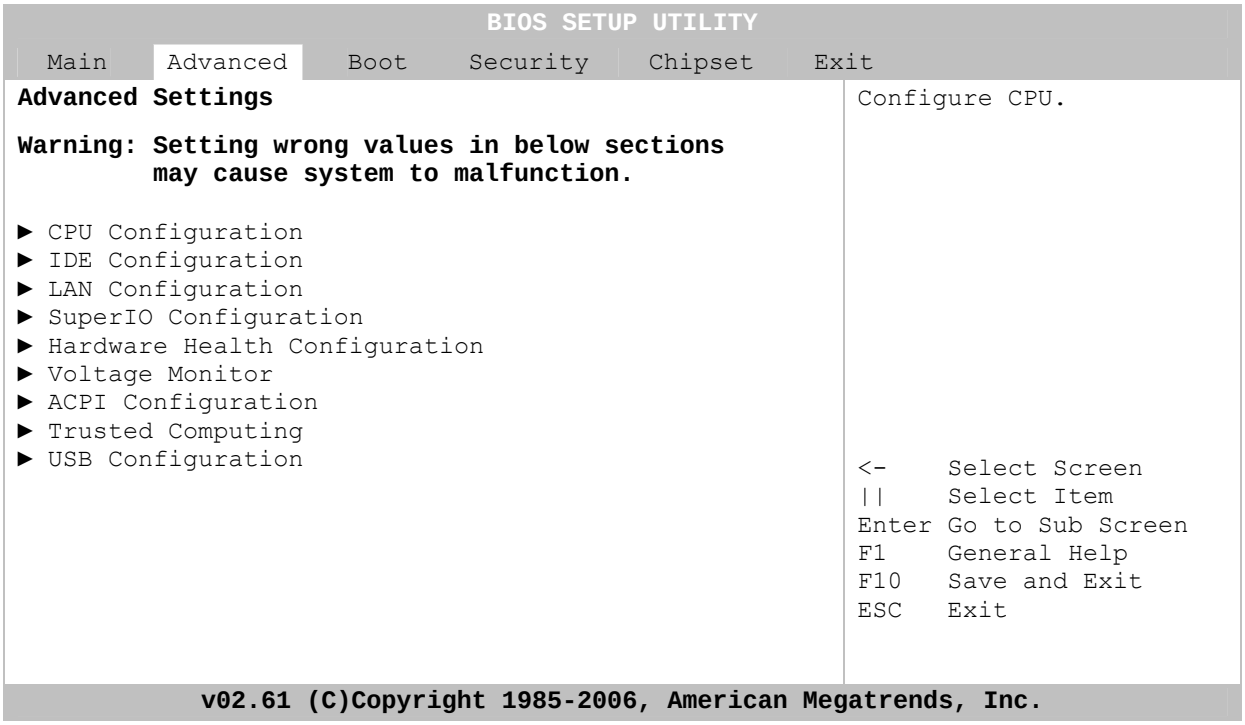


You can make the following selections. Use the sub menus for other selections.

Feature	Options	Description
System Time	HH:MM:SS	Set the system time.
System Date	MM/DD/YYYY	Set the system date.

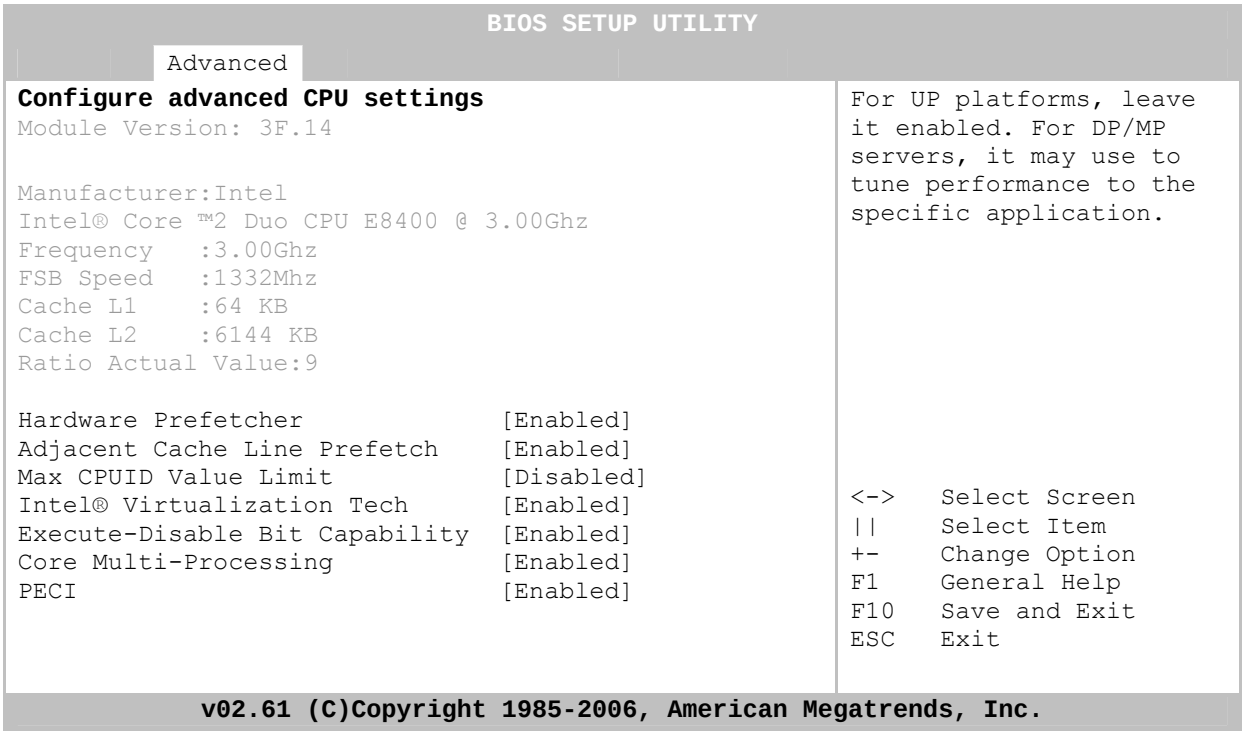
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6.6 Advanced Menu



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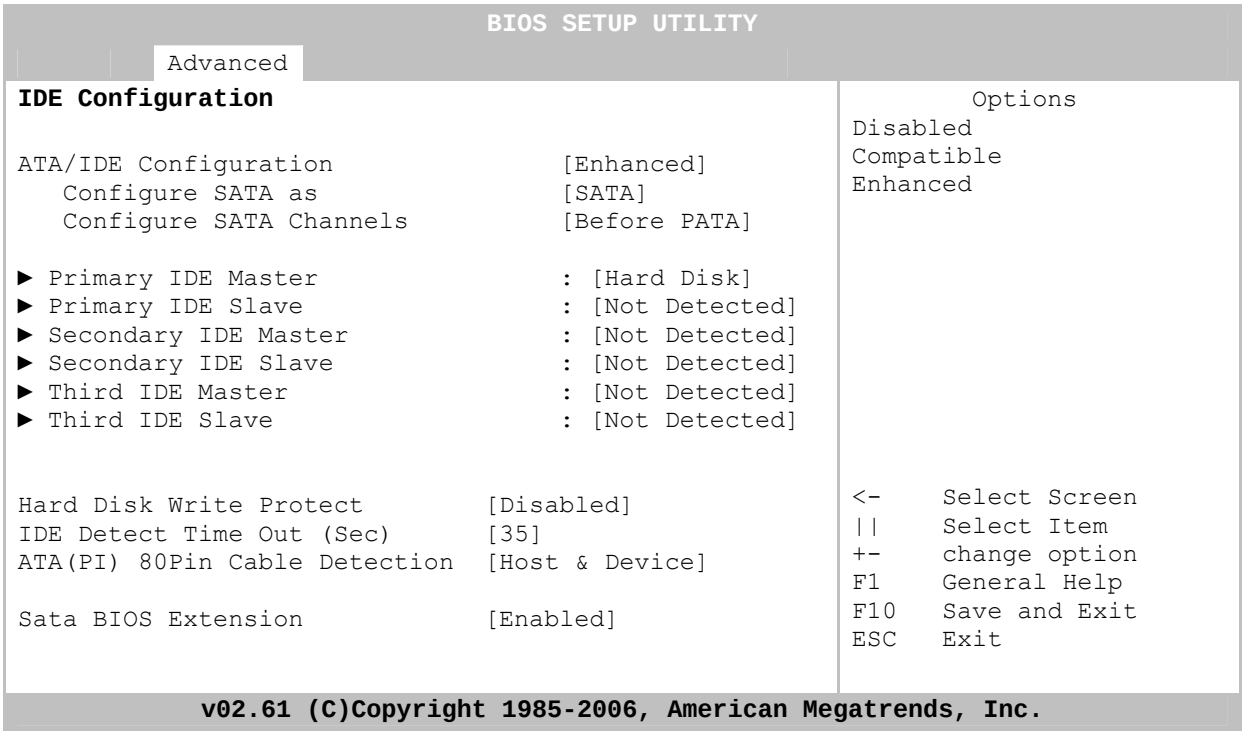
6.6.1 Advanced settings – CPU Configuration



Feature	Options	Description
Hardware Prefetcher	Disabled **Enabled**	For UP platforms, leave it enabled. For DP/MP servers it may use to tune performance to the specific application
Adjacent Cache Line Prefetch	Disabled **Enabled**	For UP platforms, leave it enabled. For DP/MP servers it may use to tune performance to the specific application
Max CPUID Value Limit	**Disabled** Enabled	Disabled for Windows XP
Intel ® Virtualization Tech	Disabled **Enabled**	When enabled, a VMM can utilize the additional HW Caps. Provided by Intel®. Virtualization Tech. Note: A full reset is required to change the setting.
Execute-Disable Bit Capability	Disabled **Enabled**	When disabled, force the XD feature flag to always return 0.
Core Multi-Processing	Disabled **Enabled**	When disabled, disable one execution core of each CPU die.
PECI	Disabled **Enabled**	When enabled, enables PECI interface.

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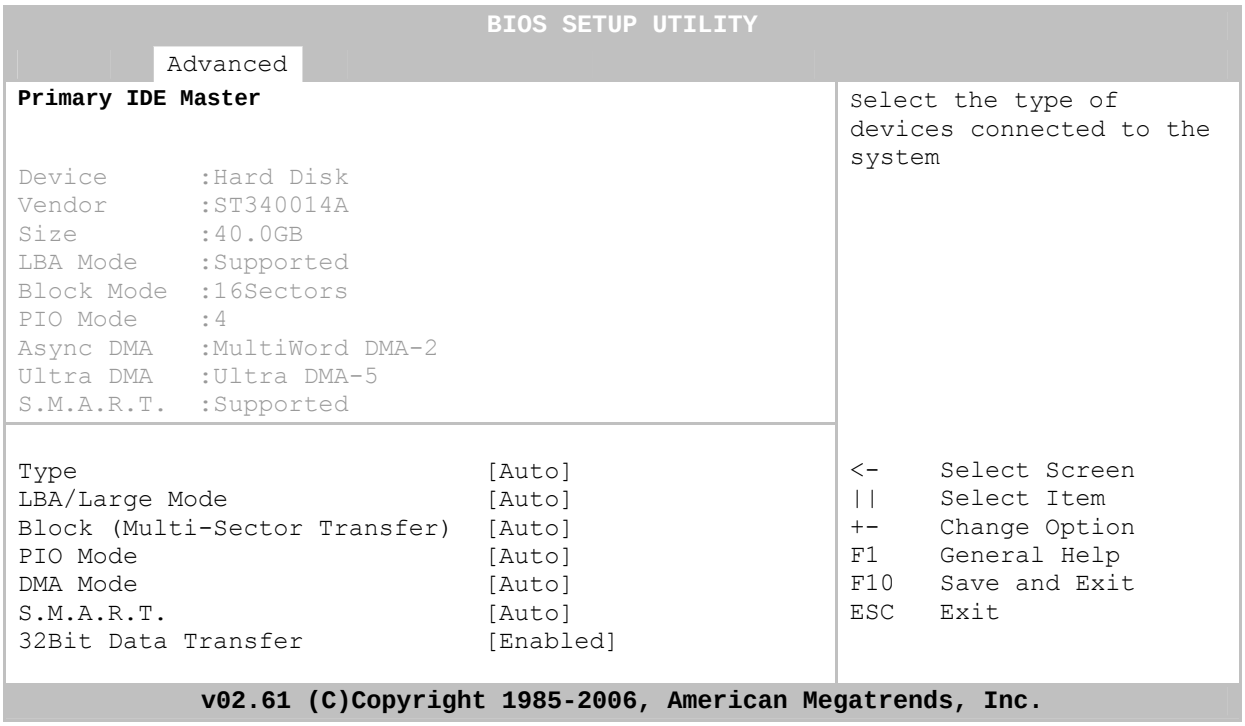
6.6.2 Advanced settings – IDE Configuration



Feature	Options	Description
ATA/IDE Configuration	Disabled Compatible **Enhanced**	Disabled Compatible Enhanced
Configure SATA as	**IDE** RAID AHCI	IDE RAID AHCI
Configure SATA Channels	**Before Pata** Behind Pata	Before Pata Behind Pata

Feature	Options	Description
Hard Disk Write Protect	**Disabled** Enabled	Disable/Enable device write protection. This will be effective only if device is accessed through BIOS
IDE Detect Time Out (Sec)	0 5 10 15 20 25 30 **35**	Select the timeout value for detecting ATA/ATAPI device(s)
Sata BIOS Extension	Disabled **Enabled**	Disabled Enabled

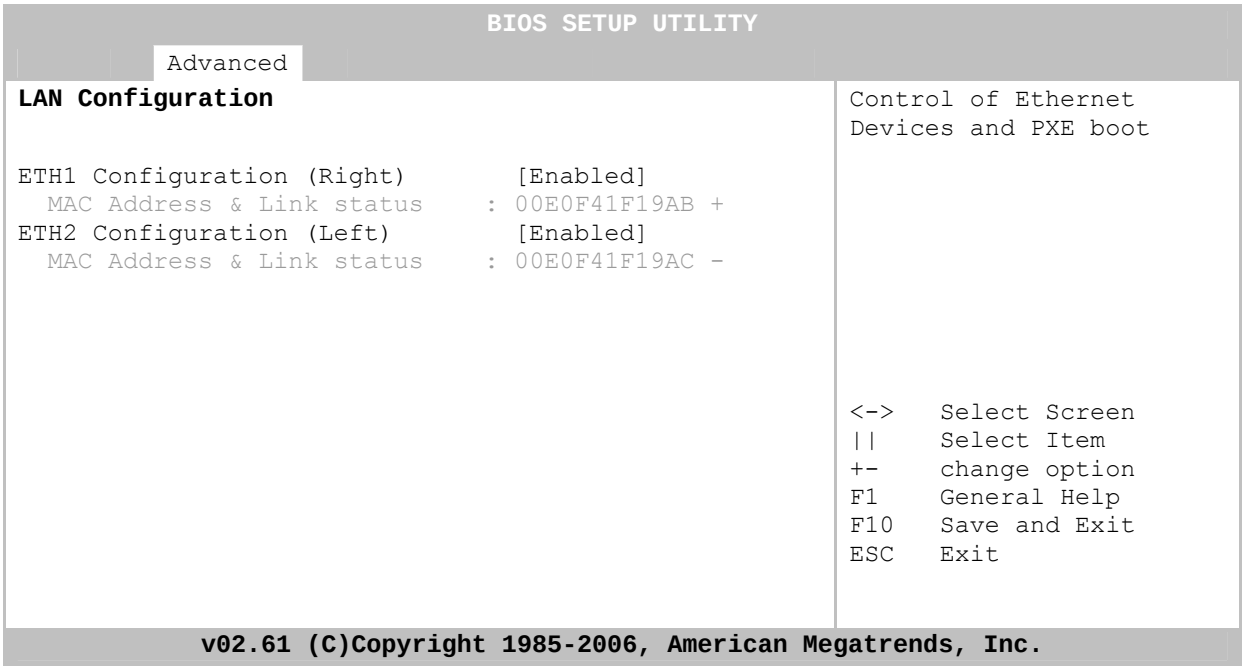
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Feature	Options	Description
Type	Not Installed **Auto** CD/DVD ARMD	Select the type of device installed
LBA/Large Mode	Disabled **Auto**	Enabling LBA causes Logical Block Addressing to be used in place of Cylinders, Heads, and Sectors.
Block (Multi-Sector Transfer)	Disabled **Auto**	Select if the device should run in Block mode
PIO Mode	**Auto** 0 1 2 3 4	Selects the method for transferring the data between the hard disk and system memory. The Setup menu only lists those options supported by the drive and platform.
DMA Mode	**Auto** SWDMA0 SWDMA1 SWDMA2 MWDMA0 MWDMA1 MWDMA2 UDMA0 UDMA1 UDMA2 UDMA3 UDMA4 UDMA5 UDMA6	Selects the Ultra DMA mode used for moving data to/from the drive. Autotype the drive to select the optimum transfer mode. **Note: To use UDMA Mode 2, 3, 4, 5 and 6 with a device, the harddisk cable used MUST be UDMA66/100 cable (80-conductor cable).**
S.M.A.R.T.	**Auto** Disabled Enabled	Select if the Device should be monitoring itself (Self-Monitoring, Analysis and Reporting Technology System)
32Bit Data Transfer	Disabled* **Enabled**	Select if the Device should be using 32Bit data Transfer

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6.6.3 Advanced settings – LAN Configuration



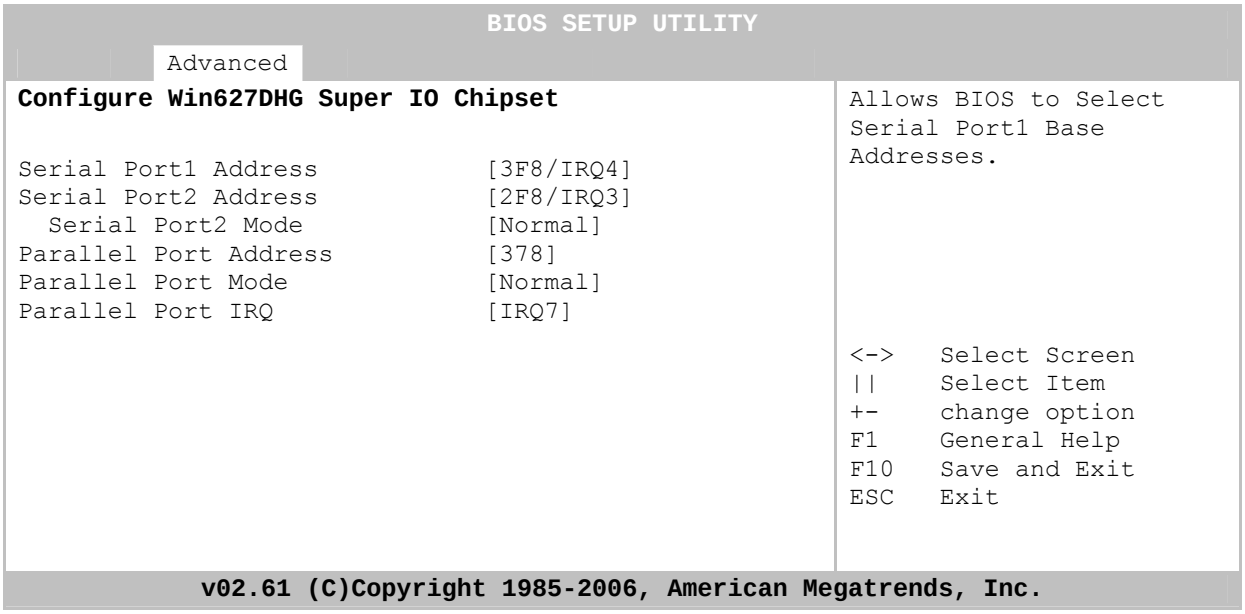
Feature	Options	Description
ETH1 Configuration	Disabled **Enabled** With RPL/PXE boot	Disable/enable LAN or enabled with RPL/PXE boot

Feature	Options	Description
ETH2 Configuration	Disabled **Enabled** With RPL/PXE boot	Disable/enable LAN or enabled with RPL/PXE boot

Note: The “+” and “-“ (to the right of the MAC address) indicates if link is established or not.

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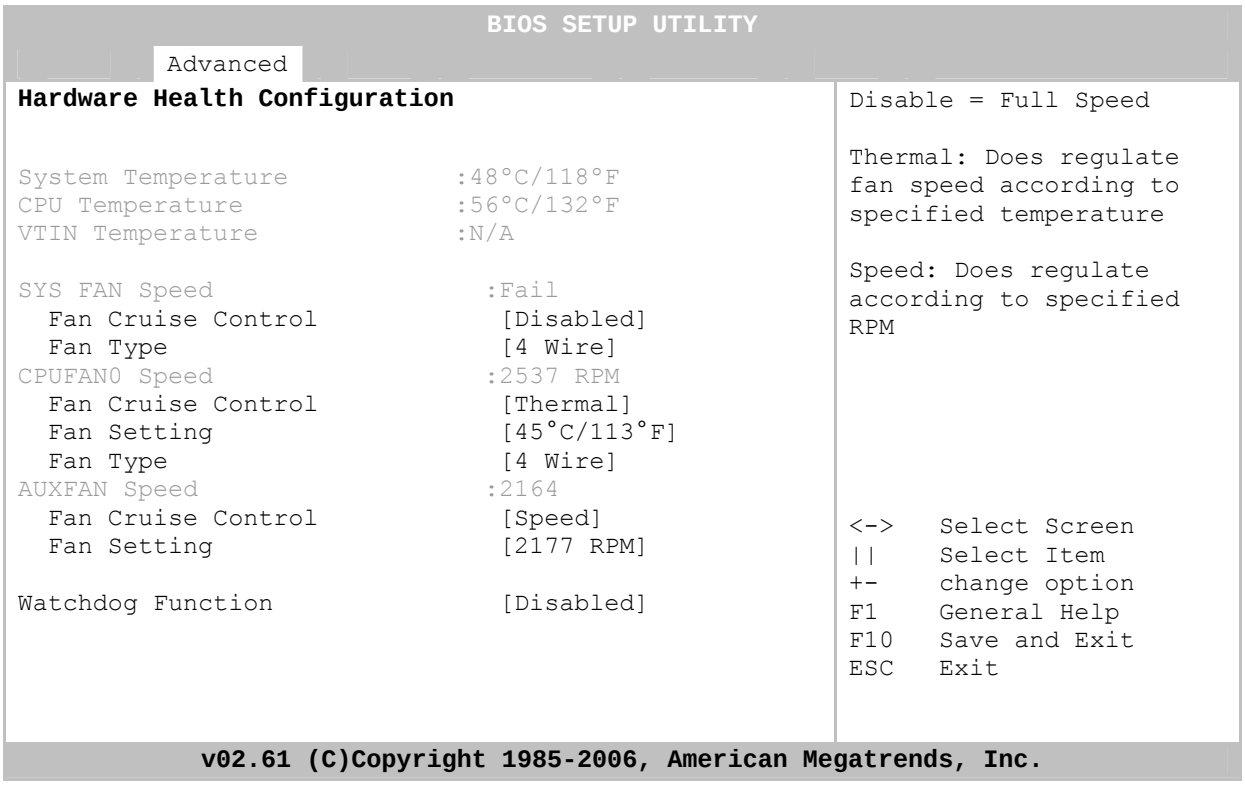
6.6.4 Advanced settings – Configure Win627DHG Super IO Chipset



Feature	Options	Description
Serial Port1 Address	Disabled **3F8/IRQ4** 2F8/IRQ3 3E8/IRQ4 2E8/IRQ3	Select the BASE I/O address and IRQ. (The available options depend on the setup for the other Serial Ports).
Serial Port2 Address	Disabled 3F8/IRQ4 **2F8/IRQ3** 3E8/IRQ4 2E8/IRQ3	Select the BASE I/O address and IRQ. (The available options depend on the setup for the other Serial Ports).
Serial Port2 Mode	**Normal** IrDA ASK IR	Select Mode for Serial Port2
If IrDA or ASK IR: IR Duplex Mode	Full Duplex **Half Duplex**	IrDA communication selection
Parallel Port Address	Disabled * **378** 278 3BC	Select the I/O address for the Parallel Port.
Parallel Port Mode	**Normal** Bi-Directional ECP EPP ECP & EEP	Select the mode of operation for the Parallel Port
If ECP Mode: ECP Mode DMA Channel	DMA0 DMA1 **DMA3**	Select a DMA channel in ECP mode of operation
If EPP mode: EPP Version	**1.9** 1.7	Select version of EPP in the EPP mode of operation
Parallel Port IRQ	IRQ5 **IRQ7**	Select a IRQ for the Parallel Port

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6.6.5 Advanced settings – Hardware Health Configuration

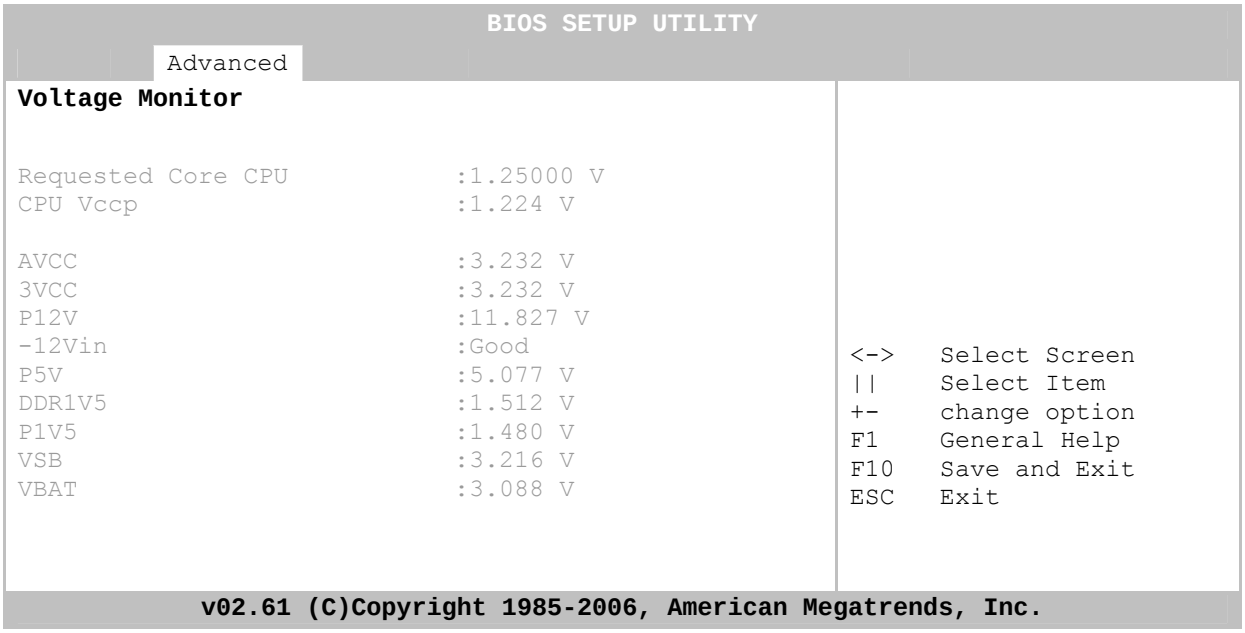


Feature	Options	Description
Fan Cruise Control	**Disabled** Thermal Speed	Select how the Fan shall operate. When set to Thermal, the Fan will start to run at the CPU die temperature set below. When set to Speed, the Fan will run at the fixed speed set below.
Fan Settings	1406-5625 RPM 30°-60°C	The fan can operate in Thermal mode or in a fixed fan speed mode
Fan Type	**4 wire** 3 wire	Select the electrical interface for the fan: (Only for CPUFAN) 3 Wire = PWM output to fan power line. RPM reading and speed regulation at lower speed might be poor. 4 Wire = 12VDC always PWM on control signal
Watchdog	**Disabled** 15 seconds 30 seconds 1 minute 2 minutes 5 minutes 10 minutes	To be serviced via API.

Note: The AUXFAN is available via Feature Connector.

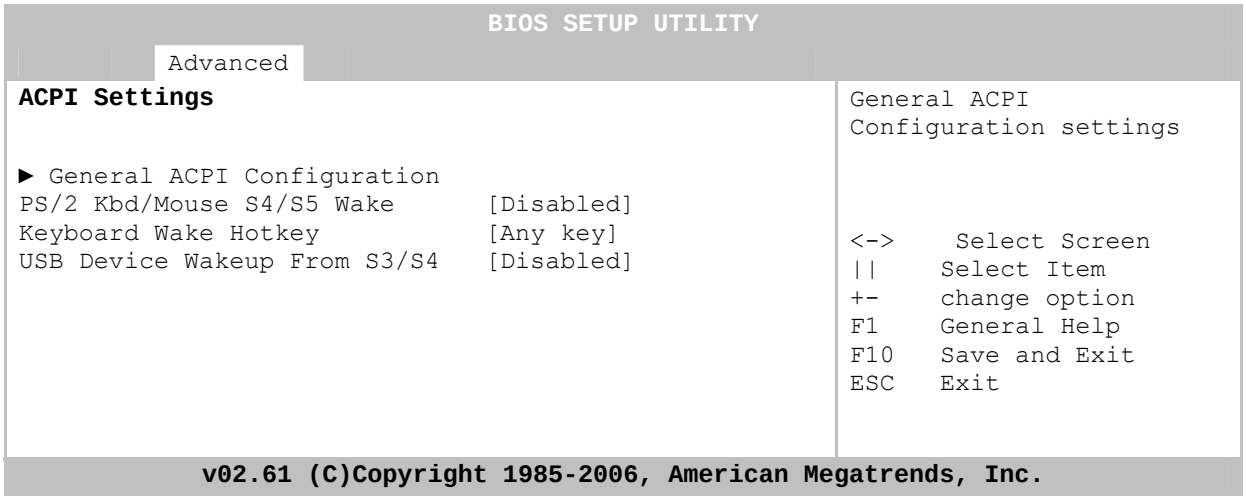
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6.6.6 Advanced settings – Voltage Monitor

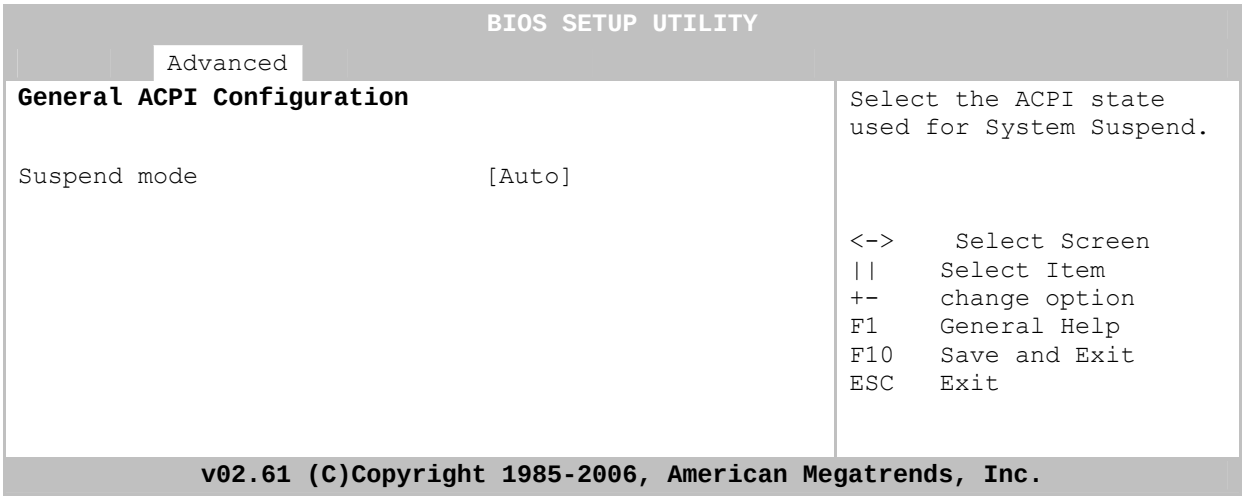


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6.6.7 Advanced settings – ACPI Settings



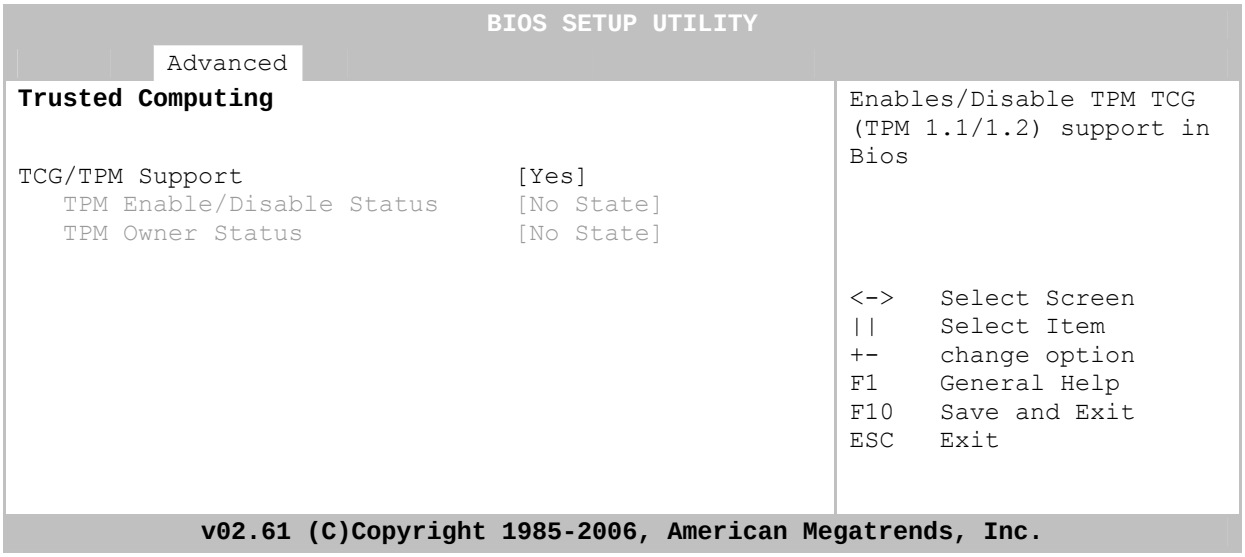
Feature	Options	Description
PS/2 Kbd/Mouse S4/S5 Wake	**Disabled** Enabled	Enabled: The System can also be waked from S4 or S5. Disabled: PS/2 Kbd or Mouse can still wake system from S3
Keyboard Wake Hotkey	**Any key** “Space” “Enter” “Sleep button”	Any key “Space” “Enter” “Sleep button”
USB Device Wakeup from S3/S4	Disabled **Enabled**	Enabled/Disable USB Device Wakeup From S3/S4.



Feature	Options	Description
Suspend mode	S1 (POS) * S3 (STR) **Auto**	Select the ACPI state used for System Suspend.

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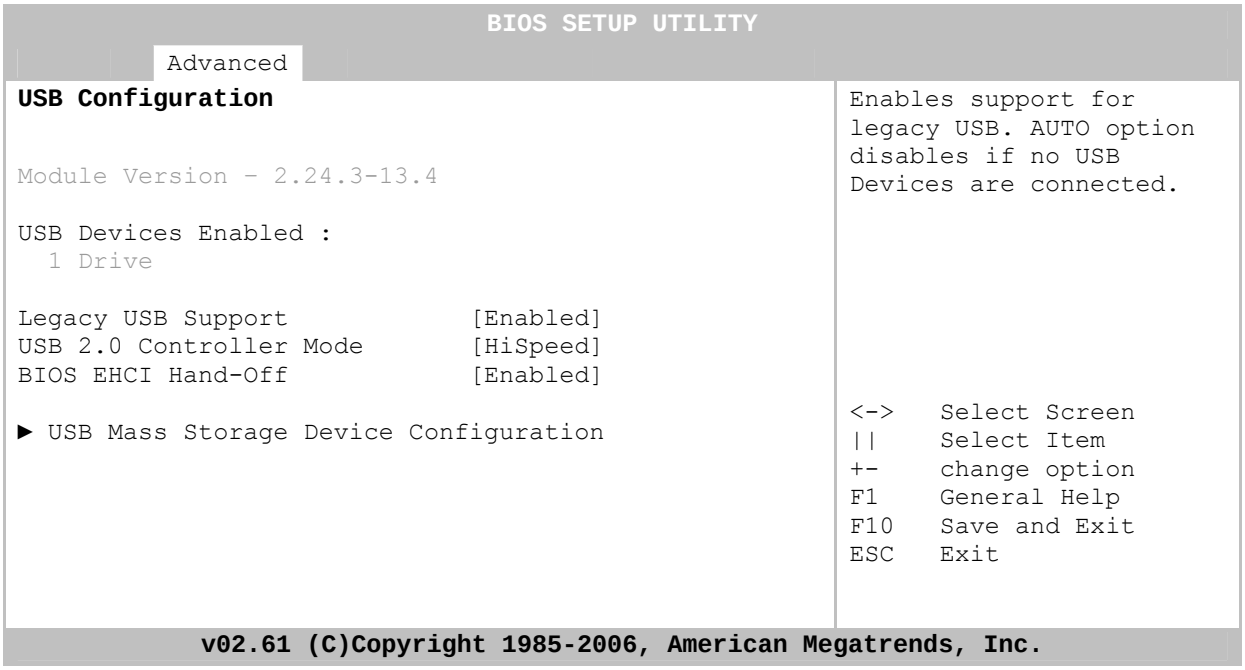
Advanced settings – Trusted Support



Feature	Options	Description
TCG/TPM Support	**No** Yes	Enables/Disable TPM TCG (TPM 1.1/1.2) Support.

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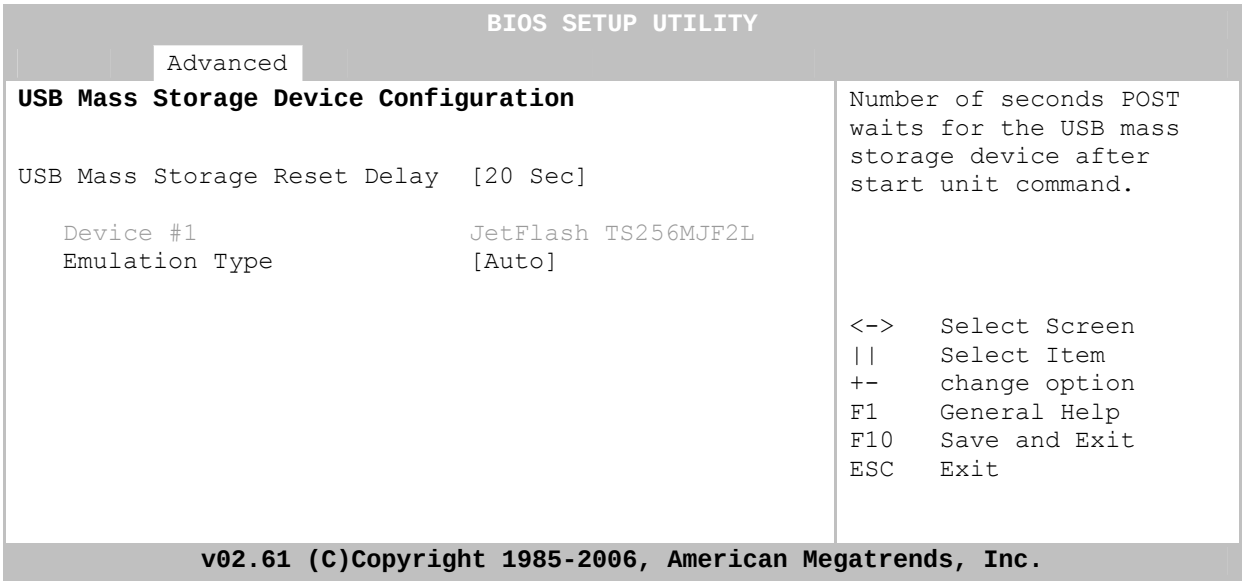
6.6.8 Advanced settings – USB Configuration



Feature	Options	Description
Legacy USB Support	Disabled **Enabled** Auto	Support for legacy USB Keyboard
USB 2.0 Controller Mode MANGLER I FAILSAFE ???	FullSpeed* **HiSpeed**	Configure the USB 2.0 controller in HiSpeed (480Mbps) or FullSpeed (12Mbps). Note: This feature is not available when Failsafe Defaults are loaded, because USB2.0 controller is disabled as default.
Bios EHCI Hand-off	Disabled **Enabled**	This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should claim by EHCI driver.

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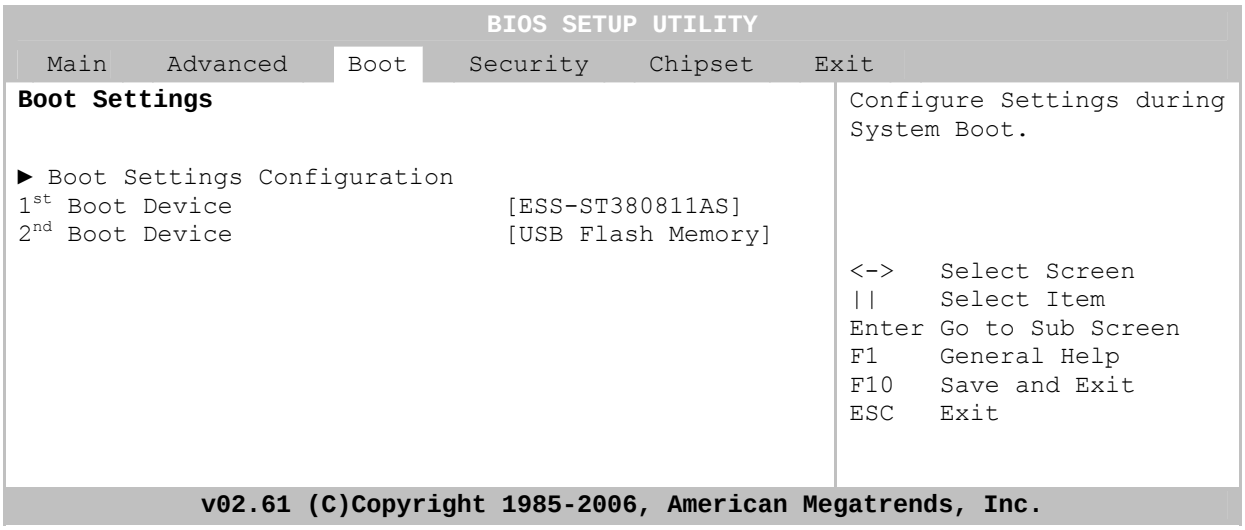
6.6.9 Advanced settings – USB Mass Storage Device Configuration



Feature	Options	Description
USB Mass Storage Reset Delay	10 Sec **20 Sec** 30 Sec 40 Sec	Number of seconds POST waits for the USB mass storage device after start unit command.
Emulation Type	**Auto** Floppy Forced FDD Hard Disk CDROM	If Auto, USB devices less than 530MB will be emulated as Floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to boot as FDD (Ex. ZIP drive).

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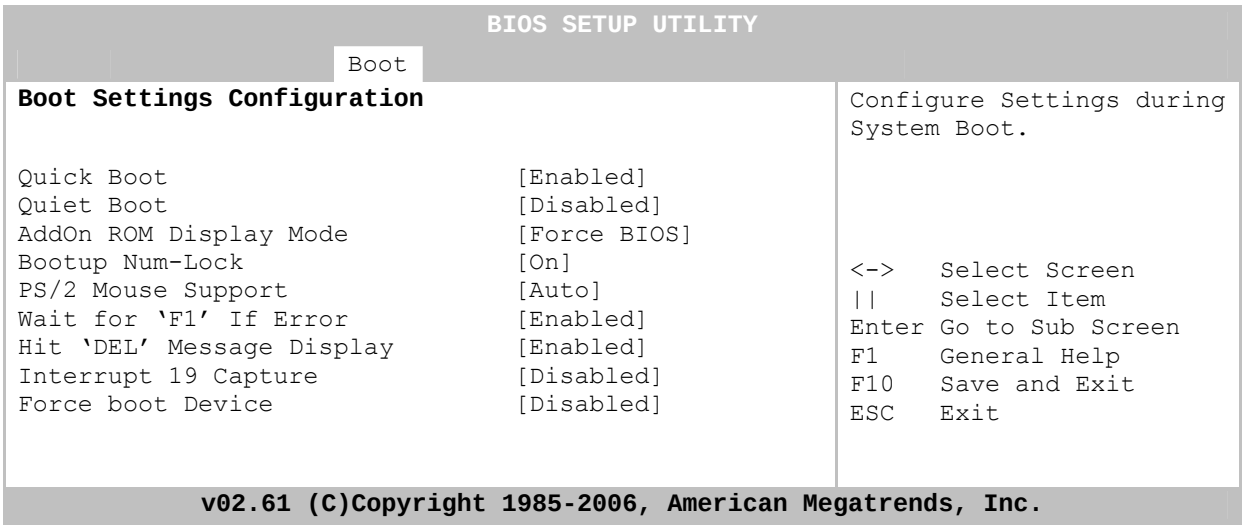
6.7 Boot Menu



Note: When pressing <F11> while booting it is possible manually to select boot device.

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6.7.1 Boot – Boot Settings Configuration



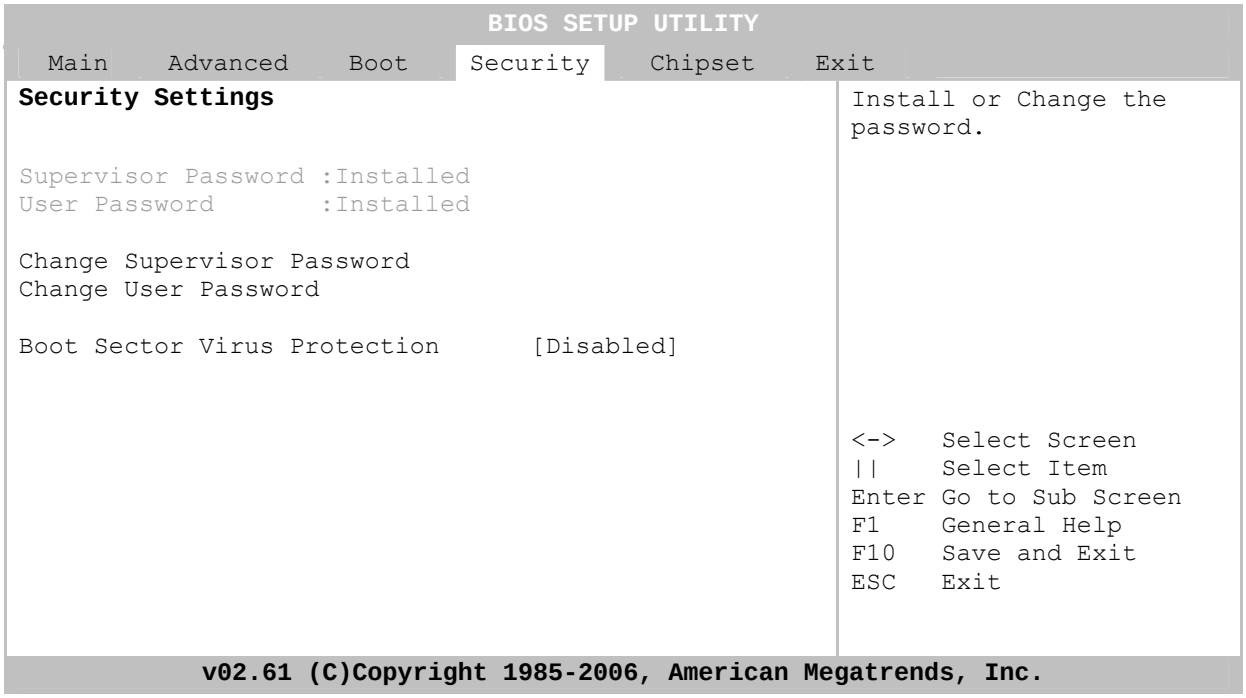
Feature	Options	Description
Quick Boot	**Enabled** Disabled	Allows BIOS to skip certain tests while booting in order to decrease boot time.
Quiet Boot	**Disabled** Enabled Black Screen White Screen	Disabled: Displays normal POST messages. Enabled: Displays OEM Logo (no POST messages). Black Screen: No picture. White Screen: White picture.
AddOn ROM Display Mode	**Force BIOS** Keep current	Set display mode for Option ROM.
Bootup Num-Lock	Off **On**	Select Power-on state for numlock
PS/2 Mouse Support	Disabled Enabled **Auto**	Select support for PS/2 Mouse.
Wait for 'F1' If Error (see note)	Disabled **Enabled**	Wait for F1 key to be pressed if error occurs.
Hit 'DEL' Message Display	Disabled **Enabled**	Displays "Press DEL to run Setup" in POST.
Interrupt 19 Capture	**Disabled** Enabled	Enabled: Allows option ROMs to trap interrupt 19
Force boot Device	**Disabled** Primary IDE Master Primary IDE Slave Secondary Sata Master Secondary Sata Slave Third IDE Master Third IDE Slave Network	Overrides current boot setting. Device must be in the boot priority menu, though. If the device fails to boot, the system will NOT try other devices.

Note: List of errors:

<INS> Pressed
Timer Error
Interrupt Controller-1 error
Keyboard/Interface Error
Halt on Invalid Time/Date
NVRAM Bad
Primary Master Hard Disk Error
S.M.A.R.T HDD Error
Cache Memory Error
DMA Controller Error
Resource Conflict
Static Resource Conflict
PCI I/O conflict
PCI ROM conflict
PCI IRQ conflict
PCI IRQ routing table error

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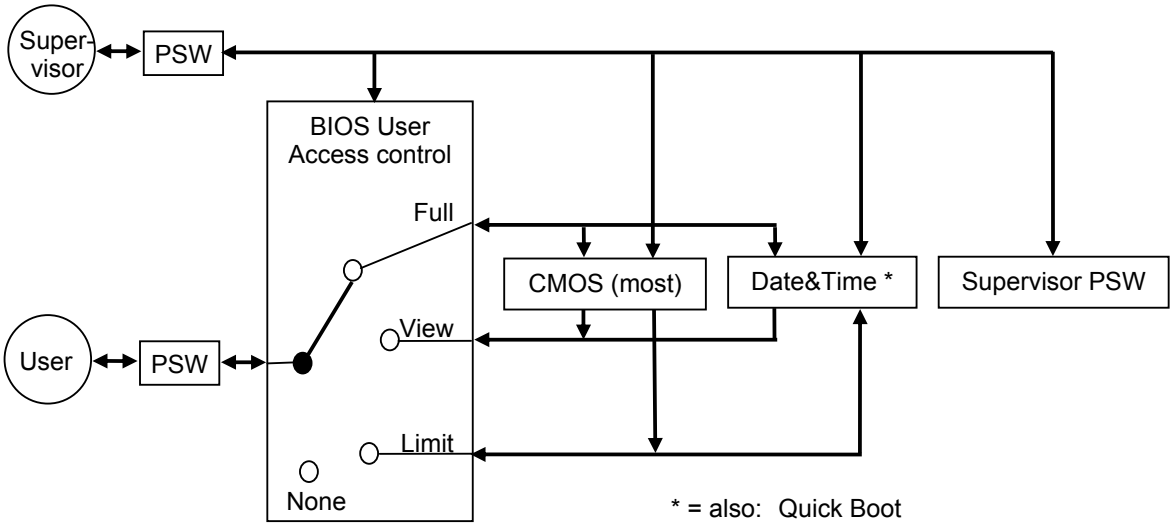
6.8 Security Menu



Feature	Options	Description
Change Supervisor Password	Password	When not cleared the advanced Supervisor Password protection system is enabled (see below diagram). Hereafter setting can only be accessed when entering BIOS as Supervisor.
User Access Level	**Full Access** View Only Limited No Access	Only visible if Supervisor Password is installed. Full Access: User can change all BIOS settings. View Only: User can only read BIOS settings. Limited: User can only read settings except: Date & Time, Quick Boot, Quiet Boot, Repost Video on S3 Resume, Active State Power-Management and Remote Access. No Access: User can not enter BIOS, but if Password Check = Always then User password will allow boot.
Change User Password	Password	Change the User Password
Password Check	**Setup** Always	Only visible if Password is installed. Setup: Protects only BIOS settings. Always: Protects both BIOS settings and Boot.
Boot Sector Virus Protection	**Disabled** Enabled	

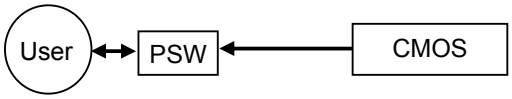
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Supervisor Password protection (setup Supervisor before User)



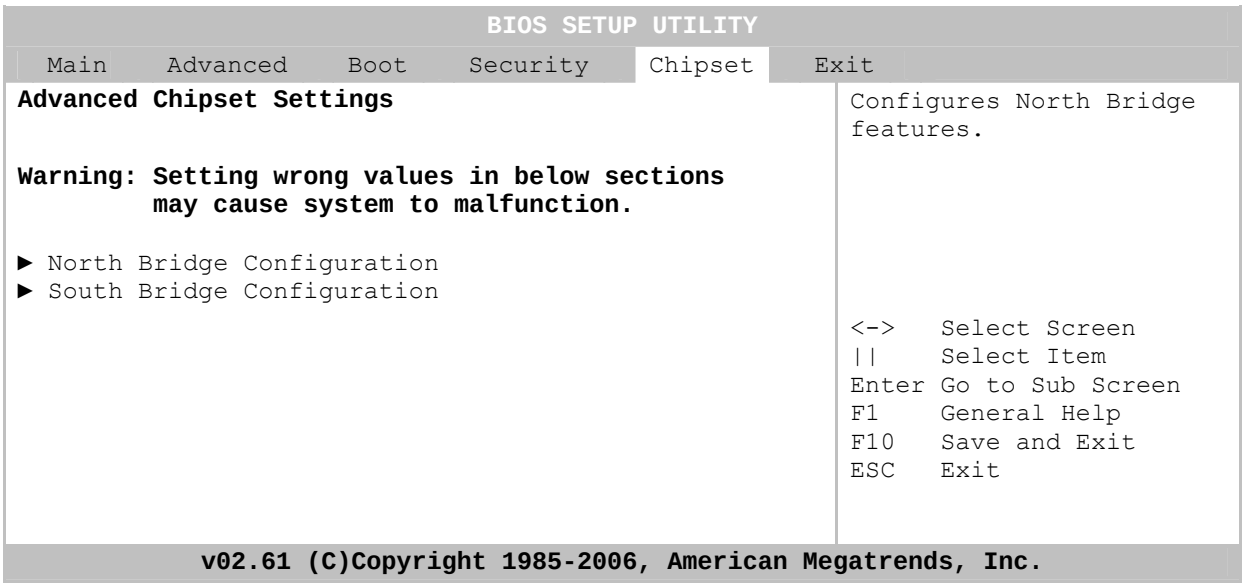
* = also: Quick Boot
Quiet Boot
Repost Video on S3 Resume
Active State Power-Management

User Password protection only (no Supervisor Password used)



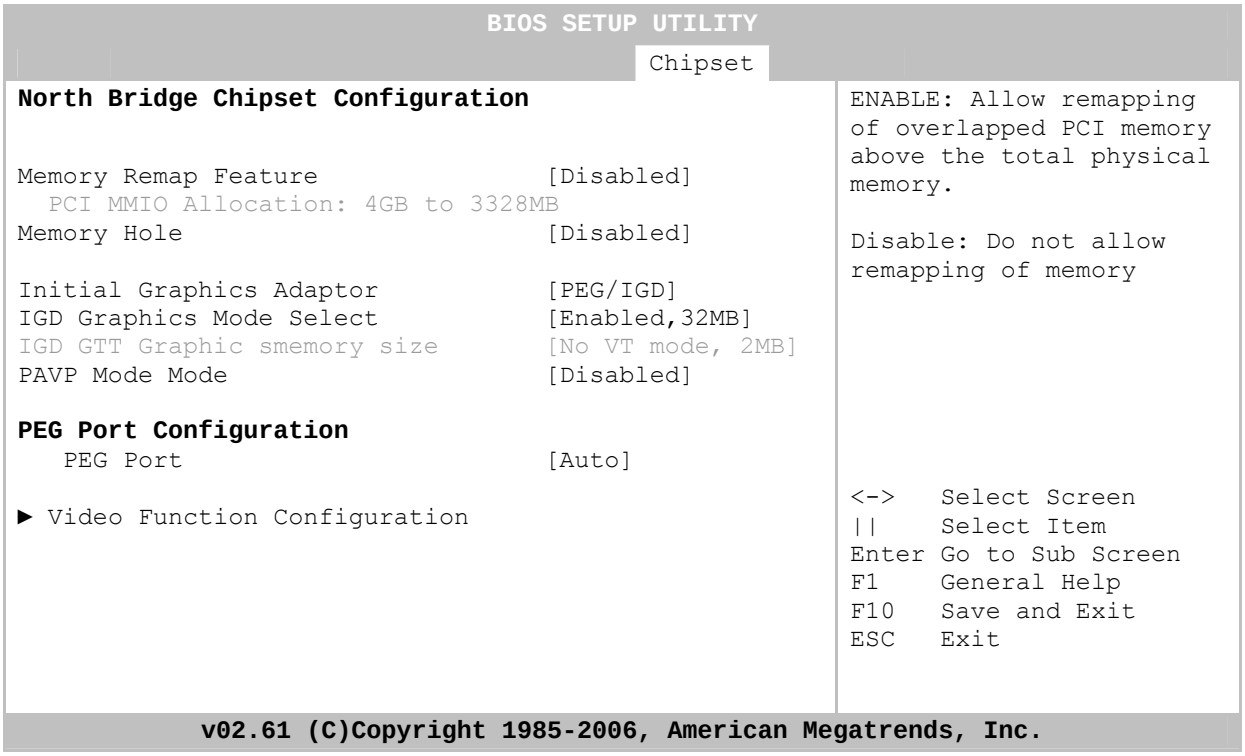
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6.9 Chipset Menu



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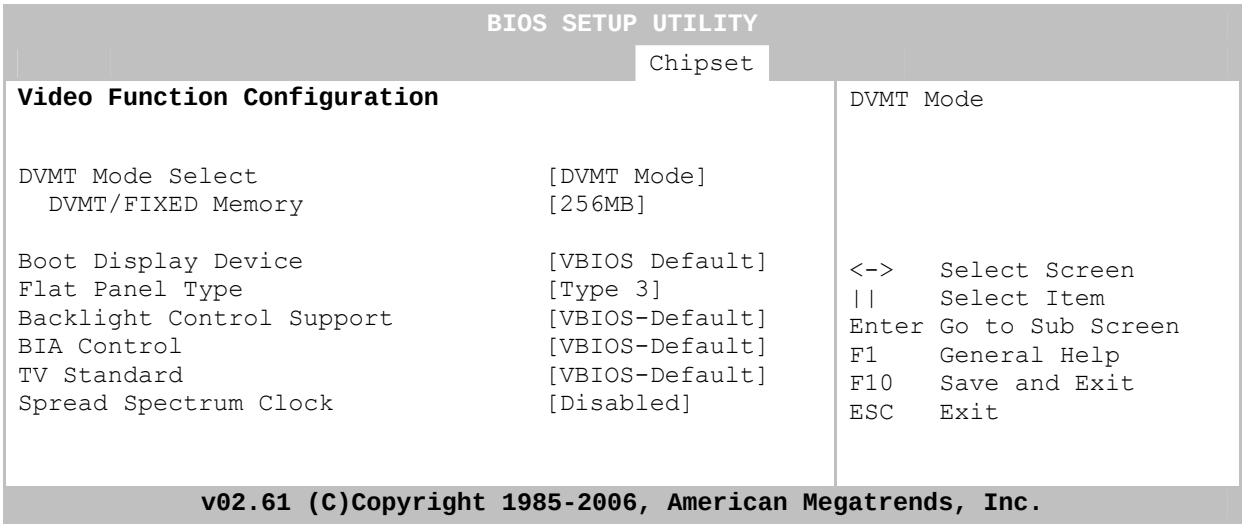
6.9.1 Advanced Chipset Settings – North Bridge Chipset Configuration



Feature	Options	Description
Memory Remap Feature	**Disabled** Enabled	ENABLE: Allow remapping of overlapped PCI memory above the total physical memory. Disable: Do not allow remapping of memory
Memory Hole	**Disabled** 15MB-16MB	**Disabled** 15MB-16MB
Initial Graphics Adaptor	IGD PCI/IGD PCI/PEG **PEG/IGD** PEG/PCI	Select which graphics controller to use as the primary boot device.
IGD Graphics Mode Select	Disabled **Enabled, 32MB** Enabled, 64MB Enabled, 128MB	Select the amount of system memory used by the Integrated Graphic Device.
PAVP Mode	**Disabled** Lite High	GMCH Protected Audio Video Path(PAVP) BIOS support.
PEG Port	**Auto** Disabled	Auto Disabled

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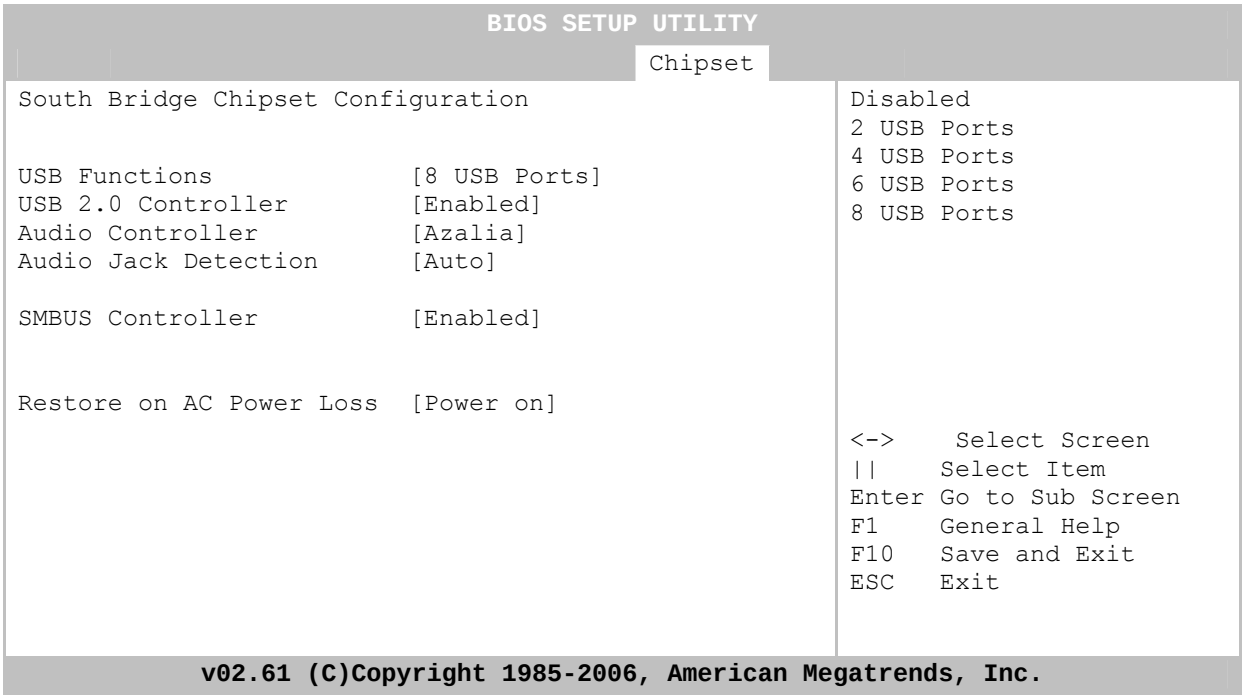
6.9.2 Advanced Chipset … – North Bridge … – Video Function Configuration



Feature	Options	Description
DVMT Mode Select	**DVMT Mode**	DVMT Mode
DVMT/FIXED Memory	128MB **256MB** Maximum DVMT	This setting is only
Boot Display Device	**VBIOS-Default** CRT TV CRT + TV SDVO CRT + SDVO LVDS CRT + LVDS	VBIOS-Default CRT TV CRT + TV SDVO CRT + SDVO LVDS CRT + LVDS
Flat Panel Type	Type 1, 2, **3**, 4 ...16	Type 1,2,3 to 16
Backlight Control Support	**VBIOS-Default** Both BLC & BIA Disabled BLC Enabled	VBIOS-Default Both BLC & BIA Disabled BLC Enabled.
BIA Control	**VBIOS-Default** BIA Disabled BIA Enabled at Level1 BIA Enabled at Level2 BIA Enabled at Level3 BIA Enabled at Level4 BIA Enabled at Level5	VBIOS-Default BIA Disabled BIA Enabled at Level1 BIA Enabled at Level2 BIA Enabled at Level3 BIA Enabled at Level4 BIA Enabled at Level5
TV Standard	**VBIOS-Default** NTSC PAL SECAM SMPTE240M ITU-R television SMPTE295M SMPTE296M EIA-770.2 EIA-770.3	VBIOS-Default NTSC PAL SECAM SMPTE240M ITU-R television SMPTE295M SMPTE296M EIA-770.2 EIA-770.3
Spread Spectrum	**Disabled** Enabled	Disabled Enabled

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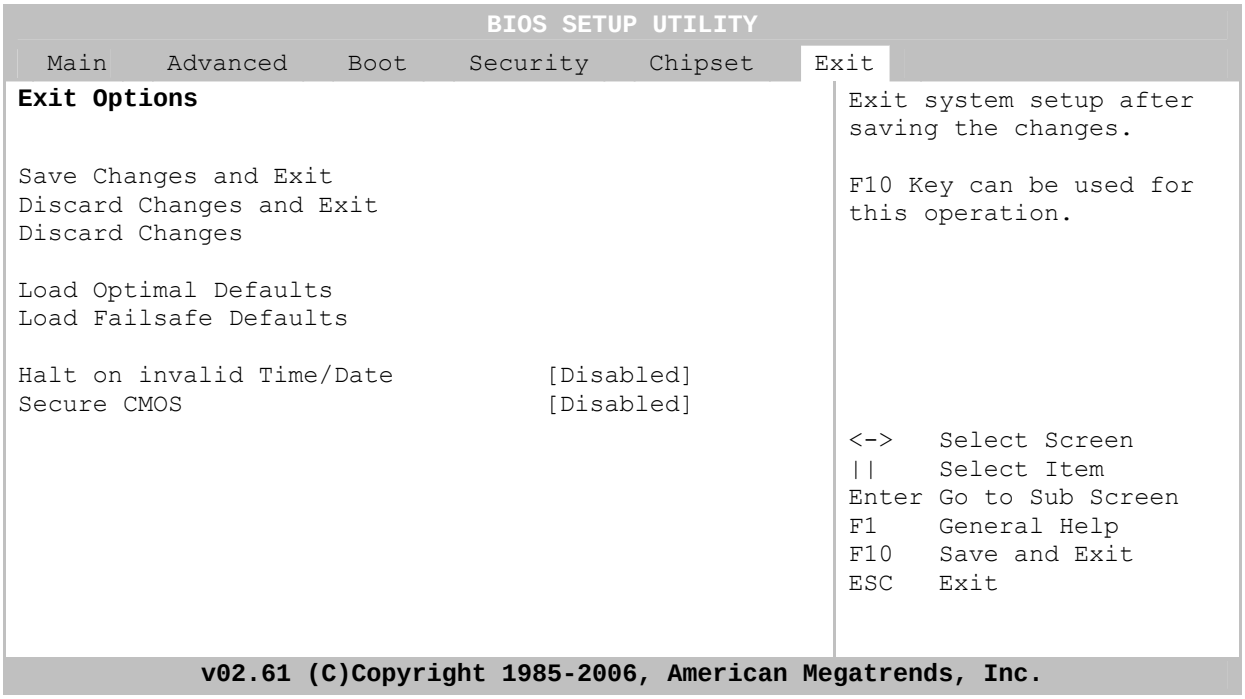
6.9.3 Advanced Chipset … – South Bridge Chipset Configuration



Feature	Options	Description
USB Functions	Disabled 2 USB Ports 4 USB Ports 6 USB Ports **8 USB Ports**	Disabled 2 USB Ports 4 USB Ports 6 USB Ports 8 USB Ports
USB 2.0 Controller	Disabled * **Enabled**	If above function “USB Function” = 10 or 12 USB Ports then USB 2.0 Controller is always enabled
Audio Controller	**Azalia** Auto * AC’97 Audio and Modem All Disabled	If above function “USB Function” = 10 or 12 USB Ports then USB 2.0 Controller is always enabled
Audio Jack Detection	Auto **Disable**	Auto: The insertion of audio jacks is auto determined. Disabled: Driver assumes that all jacks are inserted (useful when using Audio pinrow)
SMBUS Controller	**Enabled** Disabled	Disabled Enabled
Restore on AC Power Loss	Power Off **Power On** Last State	Power Off Power On Last State

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6.10 Exit Menu



Feature	Options	Description
Save Changes and Exit	Ok Cancel	Exit system setup after saving the changes
Discard Changes and Exit	Ok Cancel	Exit system setup without saving any changes
Discard Changes	Ok Cancel	Discards changes done so far to any of the setup questions
Load Optimal Defaults	Ok Cancel	Load Optimal Default values for all the setup questions
Load Failsafe Defaults	Ok Cancel	Load Failsafe Default values for all the setup questions
Halt on invalid Time/Date	Enabled **Disabled**	Enabled: System halt if incorrect Date & Time.
Secure CMOS	Enabled **Disabled**	Enable will store current CMOS in non volatile ram. (For protection of CMOS data in case of battery failure etc.)

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7 AMI BIOS Beep Codes

Boot Block Beep Codes:

Number of Beeps	Description
1	Insert diskette in floppy drive A:
2	'AMIBOOT.ROM' file not found in root directory of diskette in A:
3	Base Memory error
4	Flash Programming successful
5	Floppy read error
6	Keyboard controller BAT command failed
7	No Flash EPROM detected
8	Floppy controller failure
9	Boot Block BIOS checksum error
10	Flash Erase error
11	Flash Program error
12	'AMIBOOT.ROM' file size error
13	BIOS ROM image mismatch (file layout does not match image present in flash device)

POST BIOS Beep Codes:

Number of Beeps	Description
1	Memory refresh timer error.
2	Parity error in base memory (first 64KB block)
3	Base memory read/write test error
4	Motherboard timer not operational
5	Processor error
6	8042 Gate A20 test error (cannot switch to protected mode)
7	General exception error (processor exception interrupt error)
8	Display memory error (system video adapter)
9	AMIBIOS ROM checksum error
10	CMOS shutdown register read/write error
11	Cache memory test failed

Troubleshooting POST BIOS Beep Codes:

Number of Beeps	Troubleshooting Action
1, 2 or 3	Reset the memory, or replace with known good modules.
4-7, 9-11	Fatal error indicating a serious problem with the system. Consult your system manufacturer. Before declaring the motherboard beyond "all hope", eliminate the possibility of interference due to a malfunctioning add-in card. Remove all expansion cards, except the video adapter. • If beep codes are generated when all other expansion cards are absent, consult your system manufacturer's technical support. • If beep codes are not generated when all other expansion cards are absent, one of the add-in cards is causing the malfunction. Insert the cards back into the system one at a time until the problem happens again. This will reveal the malfunctioning card.
8	If the system video adapter is an add-in card, replace or reset the video adapter. If the video adapter is an integrated part of the system board, the board may be faulty.

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8 OS Setup

Use the Setup.exe files for all relevant drivers. The drivers can be found on KTG41 Driver CD or they can be downloaded from the homepage http://www.kontron.com/

Note: When installing Intel ® Graphics drivers it is possible for the OS to start up without any connected display(s) active. If you are able to pass on possible "Log On" etc. by entering User and Password etc. without actually seeing the picture on the display and if the Hot Keys have not been disabled in the Intel Graphic driver, then the following key combinations you can select a connected display:

9 Warranty

KONTRON Technology warrants its products to be free from defects in material and workmanship during the warranty period. If a product proves to be defective in material or workmanship during the warranty period, KONTRON Technology will, at its sole option, repair or replace the product with a similar product. Replacement Product or parts may include remanufactured or refurbished parts or components.

The warranty does not cover:

1. Damage, deterioration or malfunction resulting from:
   A. Accident, misuse, neglect, fire, water, lightning, or other acts of nature, unauthorized product modification, or failure to follow instructions supplied with the product.
   B. Repair or attempted repair by anyone not authorized by KONTRON Technology.
   C. Causes external to the product, such as electric power fluctuations or failure.
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   E. Any other causes which does not relate to a product defect.
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